Colour Television

Chassis

Q549.2E

LA

Service
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Service

Service Manual

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Subject to modification EN 3122 785 18311

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PHILIPS

1. Revision List

Manual xxxx xxx xxxx.0

- First release.

Manual xxxx xxx xxxx.1

- **All Chapters:** the following sets to the manual: see Table 2-1 Described Model numbers.
- **Chapter 5:** paragraph 5.8.10 PCI bus added.
- **Chapter 6:** paragraph 6.6 Service SSB delivered without main software loaded added.

2. Technical Specifications and, Connections

Index of this chapter:

Notes:

- Figures can deviate due to the different set executions.
- Specifications are indicative (subject to change).

2.1 Technical Specifications

For on-line product support please use the links in Table 2-1. Here is product information available, as well as getting started, user manuals, frequently asked questions and software & drivers.

Table 2-1 Described Model numbers

CTN	Styling	Published in:
32PFL9604H/12	Elite Core	3122 785 18310
32PFL9604H/60		3122 785 18310
37PFL9604H/12		3122 785 18310
37PFL9604H/60		3122 785 18311
56PFL9954H/12		3122 785 18311

2.2 Directions for Use

You can download this information from the following websites:
http://www.philips.com/support
http://www.p4c.philips.com

2.3 Connections

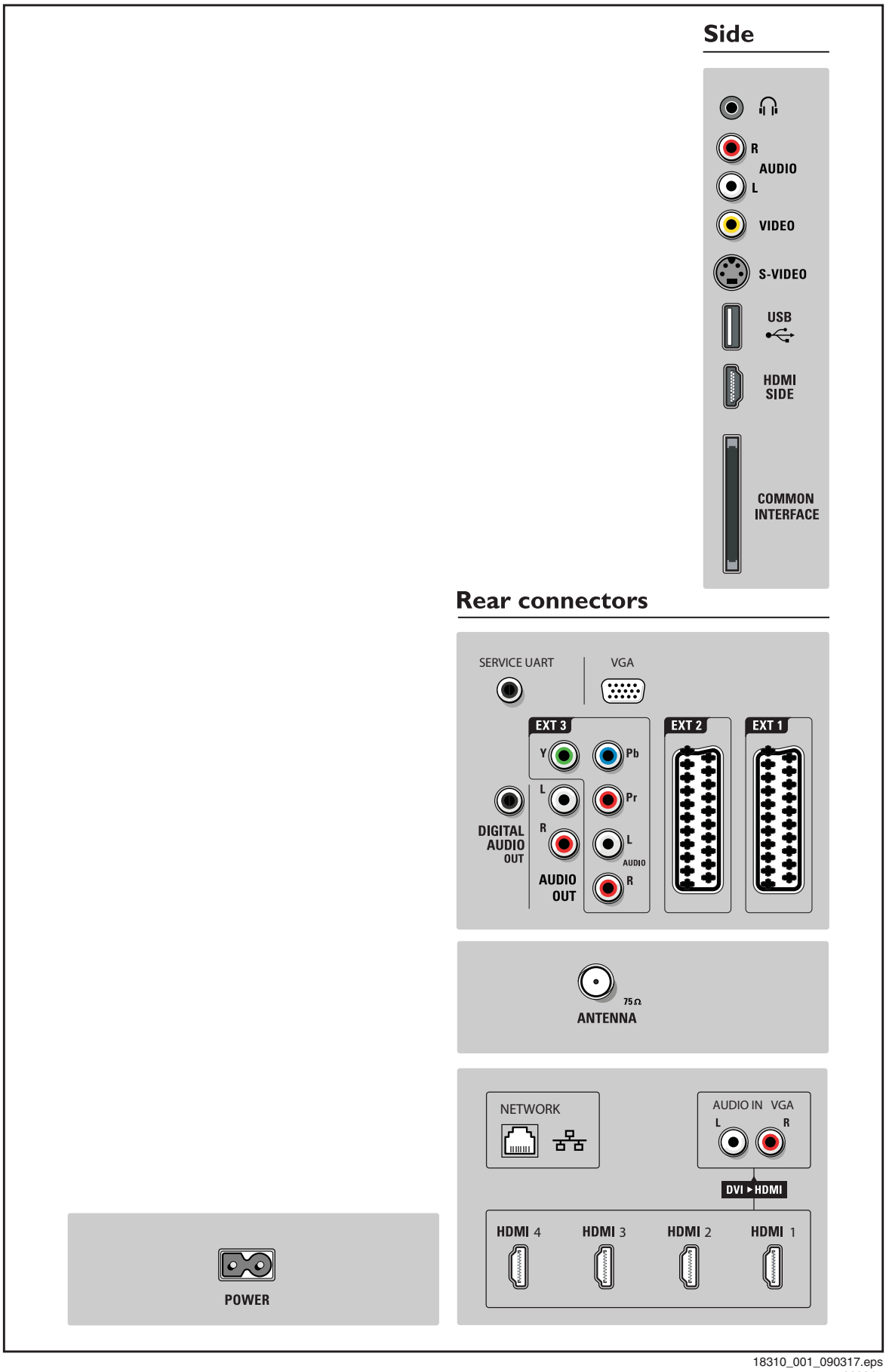

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Figure 2-1 Connection overview

Note: The following connector colour abbreviations are used (acc. to DIN/IEC 757): Bk= Black, Bu= Blue, Gn= Green, Gy= Grey, Rd= Red, Wh= White, Ye= Yellow.

2.3.1 Side Connections

Head phone (Output)

Bk	- Head phone	32 - 600 ohm / 10 mW

Cinch: Video CVBS - In, Audio - In

Rd	- Audio R	0.5 V_{RMS} / 10 kohm
Wh	- Audio L	0.5 V_{RMS} / 10 kohm
Ye	- Video CVBS	1 V_{PP} / 75 ohm

S-Video (Hosiden): Video Y/C - In

1	- Ground Y	Gnd
2	- Ground C	Gnd
3	- Video Y	1 V_{PP} / 75 ohm
4	- Video C	0.3 V_{PP} / 75 ohm

USB2.0

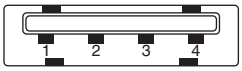

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Figure 2-2 USB (type A)

1	- +5V	
2	- Data (-)	
3	- Data (+)	
4	- Ground	Gnd

HDMI: Digital Video, Digital Audio - In
(see HDMI 1, 2, 3 & 4 - Rear Connections)

Common Interface

68p - See diagram B07A SSB: CI: PCMCIA Connector

2.3.2 Rear Connections

Service Connector (UART)

1	- Ground	Gnd
2	- UART_TX	Transmit
3	- UART_RX	Receive

VGA: Video RGB - In

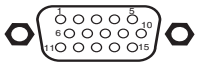

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Figure 2-3 VGA Connector

1	- Video Red	0.7 V_{PP} / 75 ohm
2	- Video Green	0.7 V_{PP} / 75 ohm
3	- Video Blue	0.7 V_{PP} / 75 ohm
4	- n.c.	
5	- Ground	Gnd
6	- Ground Red	Gnd
7	- Ground Green	Gnd
8	- Ground Blue	Gnd
9	- +5V_{DC}	+5 V
10	- Ground Sync	Gnd
11	- n.c.	
12	- DDC_SDA	DDC data
13	- H-sync	0 - 5 V
14	- V-sync	0 - 5 V
15	- DDC_SCL	DDC clock

Cinch: S/PDIF - Out

Bk	- Coaxial	0.4 - 0.6V_{PP} / 75 ohm

Cinch: Audio - Out

Rd	- Audio - R	0.5 V_{RMS} / 10 kohm
Wh	- Audio - L	0.5 V_{RMS} / 10 kohm

EXT3: Cinch: Video YPbPr - In, Audio - In

Gn	- Video Y	1 V_{PP} / 75 ohm
Bu	- Video Pb	0.7 V_{PP} / 75 ohm
Rd	- Video Pr	0.7 V_{PP} / 75 ohm
Rd	- Audio - R	0.5 V_{RMS} / 10 kohm
Wh	- Audio - L	0.5 V_{RMS} / 10 kohm

EXT1 & 2: Video RGB - In, CVBS - In/Out, Audio - In/Out

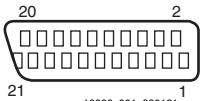

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Figure 2-4 SCART connector

1	- Audio R	0.5 V_{RMS} / 1 kohm
2	- Audio R	0.5 V_{RMS} / 10 kohm
3	- Audio L	0.5 V_{RMS} / 1 kohm
4	- Ground Audio	Gnd
5	- Ground Blue	Gnd
6	- Audio L	0.5 V_{RMS} / 10 kohm
7	- Video Blue	0.7 V_{PP} / 75 ohm
8	- Function Select	0 - 2 V: INT 4.5 - 7 V: EXT 16:9 9.5 - 12 V: EXT 4:3
9	- Ground Green	Gnd
10	- n.c.	
11	- Video Green	0.7 V_{PP} / 75 ohm
12	- n.c.	
13	- Ground Red	Gnd
14	- Ground P50	Gnd
15	- Video Red	0.7 V_{PP} / 75 ohm
16	- Status/FBL	0 - 0.4 V: INT 1 - 3 V: EXT / 75 ohm
17	- Ground Video	Gnd
18	- Ground FBL	Gnd
19	- Video CVBS/Y	1 V_{PP} / 75 ohm
20	- Video CVBS	1 V_{PP} / 75 ohm
21	- Shield	Gnd

Aerial - In

-	- IEC-type (EU)	Coax, 75 ohm

RJ45: Ethernet (if present)

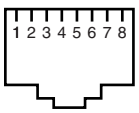

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Figure 2-5 Ethernet connector

1	- TD+	Transmit signal
2	- TD-	Transmit signal
3	- RD+	Receive signal
4	- CT	Centre Tap: DC level fixation
5	- CT	Centre Tap: DC level fixation
6	- RD-	Receive signal
7	- GND	Gnd
8	- GND	Gnd

Cinch: Audio - In (VGA/DVI)

Rd - Audio R	0.5 V_{RMS} / 10 kohm	
Wh - Audio L	0.5 V_{RMS} / 10 kohm	

HDMI 1, 2, 3 & 4: Digital Video, Digital Audio - In

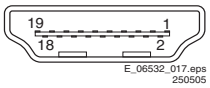

Figure 2-6 HDMI (type A) connector

1	- D2+	Data channel	
2	- Shield	Gnd	
3	- D2-	Data channel	
4	- D1+	Data channel	
5	- Shield	Gnd	
6	- D1-	Data channel	
7	- D0+	Data channel	
8	- Shield	Gnd	
9	- D0-	Data channel	
10	- CLK+	Data channel	
11	- Shield	Gnd	
12	- CLK-	Data channel	
13	- Easylink/CEC	Control channel	
14	- n.c.		
15	- DDC_SCL	DDC clock	
16	- DDC_SDA	DDC data	
17	- Ground	Gnd	
18	- +5V		
19	- HPD	Hot Plug Detect	
20	- Ground	Gnd	

2.4 Chassis Overview

Refer to chapter Block Diagrams for PWB/CBA locations.

3. Precautions, Notes, and Abbreviation List

Index of this chapter:

3.1 Safety Instructions

Safety regulations require the following **during** a repair:

- Connect the set to the Mains/AC Power via an isolation transformer (> 800 VA).
- Replace safety components, indicated by the symbol ⚠, only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard. Of de set ontploft!

Safety regulations require that **after** a repair, the set must be returned in its original condition. Pay in particular attention to the following points:

- Route the wire trees correctly and fix them with the mounted cable clamps.
- Check the insulation of the Mains/AC Power lead for external damage.
- Check the strain relief of the Mains/AC Power cord for proper function.
- Check the electrical DC resistance between the Mains/AC Power plug and the secondary side (only for sets that have a Mains/AC Power isolated power supply):
  1. Unplug the Mains/AC Power cord and connect a wire between the two pins of the Mains/AC Power plug.
  2. Set the Mains/AC Power switch to the “on” position (keep the Mains/AC Power cord unplugged!).
  3. Measure the resistance value between the pins of the Mains/AC Power plug and the metal shielding of the tuner or the aerial connection on the set. The reading should be between 4.5 MΩ and 12 MΩ.
  4. Switch “off” the set, and remove the wire between the two pins of the Mains/AC Power plug.
- Check the cabinet for defects, to prevent touching of any inner parts by the customer.

3.2 Warnings

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are connected with the same potential as the mass of the set by a wristband with resistance. Keep components and tools also at this same potential.
- Be careful during measurements in the high voltage section.
- Never replace modules or other components while the unit is switched “on”.
- When you align the set, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

3.3 Notes

3.3.1 General

- Measure the voltages and waveforms with regard to the chassis (= tuner) ground (⏚), or hot ground (⏚), depending on the tested area of circuitry. The voltages and waveforms shown in the diagrams are indicative. Measure them in the Service Default Mode with a colour bar signal and stereo sound (L: 3 kHz, R: 1 kHz unless stated otherwise) and picture carrier at 475.25 MHz for PAL, or 61.25 MHz for NTSC (channel 3).
- Where necessary, measure the waveforms and voltages with (⊓⊓) and without (⊼) aerial signal. Measure the voltages in the power supply section both in normal operation (⏻) and in stand-by (⏻). These values are indicated by means of the appropriate symbols.

3.3.2 Schematic Notes

- All resistor values are in ohms, and the value multiplier is often used to indicate the decimal point location (e.g. 2K2 indicates 2.2 kΩ).
- Resistor values with no multiplier may be indicated with either an “E” or an “R” (e.g. 220E or 220R indicates 220 Ω).
- All capacitor values are given in micro-farads ($\mu = \times 10^{-6}$), nano-farads ($n = \times 10^{-9}$), or pico-farads ($p = \times 10^{-12}$).
- Capacitor values may also use the value multiplier as the decimal point indication (e.g. 2p2 indicates 2.2 pF).
- An “asterisk” (*) indicates component usage varies. Refer to the diversity tables for the correct values.
- The correct component values are listed on the Philips Spare Parts Web Portal.

3.3.3 Spare Parts

For the latest spare part overview, consult your Philips Spare Part web portal.

3.3.4 BGA (Ball Grid Array) ICs

Introduction

For more information on how to handle BGA devices, visit this URL: http://www.atyourservice-magazine.com. Select “Magazine”, then go to “Repair downloads”. Here you will find Information on how to deal with BGA-ICs.

BGA Temperature Profiles

For BGA-ICs, you **must** use the correct temperature-profile. Where applicable and available, this profile is added to the IC Data Sheet information section in this manual.

3.3.5 Lead-free Soldering

Due to lead-free technology some rules have to be respected by the workshop during a repair:

- Use only lead-free soldering tin. If lead-free solder paste is required, please contact the manufacturer of your soldering equipment. In general, use of solder paste within workshops should be avoided because paste is not easy to store and to handle.
- Use only adequate solder tools applicable for lead-free soldering tin. The solder tool must be able:
  - To reach a solder-tip temperature of at least 400°C.
  - To stabilize the adjusted temperature at the solder-tip.
  - To exchange solder-tips for different applications.
- Adjust your solder tool so that a temperature of around 360°C - 380°C is reached and stabilized at the solder joint. Heating time of the solder-joint should not exceed ~ 4 sec. Avoid temperatures above 400°C, otherwise wear-out of tips will increase drastically and flux-fluid will be destroyed. To avoid wear-out of tips, switch “off” unused equipment or reduce heat.
- Mix of lead-free soldering tin/parts with leaded soldering tin/parts is possible but PHILIPS recommends strongly **to avoid** mixed regimes. If this cannot be avoided, carefully clear the solder-joint from old tin and re-solder with new tin.

3.3.6 Alternative BOM identification

It should be noted that on the European Service website, “Alternative BOM” is referred to as “Design variant”.

The **third digit** in the serial number (example: AG**2**B0335000001) indicates the number of the alternative B.O.M. (Bill Of Materials) that has been used for producing the specific TV set. In general, it is possible that the same TV model on the market is produced with e.g. two different types of displays, coming from two different suppliers. This will then result in sets which have the same CTN (Commercial Type Number; e.g. 28PW9515/12) but which have a different B.O.M. number.
By looking at the third digit of the serial number, one can identify which B.O.M. is used for the TV set he is working with. If the third digit of the serial number contains the number “1” (example: AG**1**B033500001), then the TV set has been manufactured according to B.O.M. number 1. If the third digit is a “2” (example: AG**2**B0335000001), then the set has been produced according to B.O.M. no. 2. This is important for ordering the correct spare parts!
For the third digit, the numbers 1...9 and the characters A...Z can be used, so in total: 9 plus 26= 35 different B.O.M.s can be indicated by the third digit of the serial number.

Identification: The bottom line of a type plate gives a 14-digit serial number. Digits 1 and 2 refer to the production centre (e.g. AG is Bruges), digit 3 refers to the B.O.M. code, digit 4 refers to the Service version change code, digits 5 and 6 refer to the production year, and digits 7 and 8 refer to production week (in example below it is 2006 week 17). The 6 last digits contain the serial number.

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Figure 3-1 Serial number (example)

3.3.7 Board Level Repair (BLR) or Component Level Repair (CLR)

If a board is defective, consult your repair procedure to decide if the board has to be exchanged or if it should be repaired on component level.
If your repair procedure says the board should be exchanged completely, do not solder on the defective board. Otherwise, it cannot be returned to the O.E.M. supplier for back charging!

3.3.8 Practical Service Precautions

- **It makes sense to avoid exposure to electrical shock.** While some sources are expected to have a possible dangerous impact, others of quite high potential are of limited current and are sometimes held in less regard.
- **Always respect voltages**. While some may not be dangerous in themselves, they can cause unexpected reactions that are best avoided. Before reaching into a powered TV set, it is best to test the high voltage insulation. It is easy to do, and is a good service precaution.

3.4 Abbreviation List

0/6/12	SCART switch control signal on A/V board. 0 = loop through (AUX to TV), 6 = play 16 : 9 format, 12 = play 4 : 3 format
AARA	Automatic Aspect Ratio Adaptation: algorithm that adapts aspect ratio to remove horizontal black bars; keeps the original aspect ratio
ACI	Automatic Channel Installation: algorithm that installs TV channels directly from a cable network by means of a predefined TXT page
ADC	Analogue to Digital Converter
AFC	Automatic Frequency Control: control signal used to tune to the correct frequency
AGC	Automatic Gain Control: algorithm that controls the video input of the feature box
AM	Amplitude Modulation
AP	Asia Pacific
AR	Aspect Ratio: 4 by 3 or 16 by 9
ASF	Auto Screen Fit: algorithm that adapts aspect ratio to remove horizontal black bars without discarding video information
ATSC	Advanced Television Systems Committee, the digital TV standard in the USA
ATV	See Auto TV
Auto TV	A hardware and software control system that measures picture content, and adapts image parameters in a dynamic way
AV	External Audio Video
AVC	Audio Video Controller
AVIP	Audio Video Input Processor
B/G	Monochrome TV system. Sound carrier distance is 5.5 MHz
BLR	Board-Level Repair
BTSC	Broadcast Television Standard Committee. Multiplex FM stereo sound system, originating from the USA and used e.g. in LATAM and AP-NTSC countries
B-TXT	Blue TeleteXT
C	Centre channel (audio)
CEC	Consumer Electronics Control bus: remote control bus on HDMI connections
CL	Constant Level: audio output to connect with an external amplifier
CLR	Component Level Repair
ComPair	Computer aided rePair
CP	Connected Planet / Copy Protection
CSM	Customer Service Mode
CTI	Color Transient Improvement: manipulates steepness of chroma transients
CVBS	Composite Video Blanking and Synchronization
DAC	Digital to Analogue Converter
DBE	Dynamic Bass Enhancement: extra low frequency amplification
DDC	See “E-DDC”
D/K	Monochrome TV system. Sound carrier distance is 6.5 MHz
DFI	Dynamic Frame Insertion
DFU	Directions For Use: owner's manual
DMR	Digital Media Reader: card reader
DMSD	Digital Multi Standard Decoding
DNM	Digital Natural Motion

DNR	Digital Noise Reduction: noise reduction feature of the set
DRAM	Dynamic RAM
DRM	Digital Rights Management
DSP	Digital Signal Processing
DST	Dealer Service Tool: special remote control designed for service technicians
DTCP	Digital Transmission Content Protection; A protocol for protecting digital audio/video content that is traversing a high speed serial bus, such as IEEE-1394
DVB-C	Digital Video Broadcast - Cable
DVB-T	Digital Video Broadcast - Terrestrial
DVD	Digital Versatile Disc
DVI(-d)	Digital Visual Interface (d= digital only)
E-DDC	Enhanced Display Data Channel (VESA standard for communication channel and display). Using E-DDC, the video source can read the EDID information form the display.
EDID	Extended Display Identification Data (VESA standard)
EEPROM	Electrically Erasable and Programmable Read Only Memory
EMI	Electro Magnetic Interference
EPLD	Erasable Programmable Logic Device
EU	Europe
EXT	EXTernal (source), entering the set by SCART or by cinches (jacks)
FDS	Full Dual Screen (same as FDW)
FDW	Full Dual Window (same as FDS)
FLASH	FLASH memory
FM	Field Memory or Frequency Modulation
FPGA	Field-Programmable Gate Array
FTV	Flat TeleVision
Gb/s	Giga bits per second
G-TXT	Green TeleteXT
H	H_sync to the module
HD	High Definition
HDD	Hard Disk Drive
HDCP	High-bandwidth Digital Content Protection: A “key” encoded into the HDMI/DVI signal that prevents video data piracy. If a source is HDCP coded and connected via HDMI/DVI without the proper HDCP decoding, the picture is put into a “snow vision” mode or changed to a low resolution. For normal content distribution the source and the display device must be enabled for HDCP “software key” decoding.
HDMI	High Definition Multimedia Interface
HP	HeadPhone
I	Monochrome TV system. Sound carrier distance is 6.0 MHz
I^2C	Inter IC bus
I^2D	Inter IC Data bus
I^2S	Inter IC Sound bus
IF	Intermediate Frequency
IR	Infra Red
IRQ	Interrupt Request
ITU-656	The ITU Radio communication Sector (ITU-R) is a standards body subcommittee of the International Telecommunication Union relating to radio communication. ITU-656 (a.k.a. SDI), is a digitized video format used for broadcast grade video. Uncompressed digital component or digital composite signals can be used. The SDI signal is self-synchronizing, uses 8 bit or 10 bit data words, and has a maximum data rate of 270 Mbit/s, with a minimum bandwidth of 135 MHz.
ITV	Institutional TeleVision; TV sets for hotels, hospitals etc.
LS	Last Status; The settings last chosen by the customer and read and stored in RAM or in the NVM. They are called at start-up of the set to configure it according to the customer's preferences
LATAM	Latin America
LCD	Liquid Crystal Display
LED	Light Emitting Diode
L/L'	Monochrome TV system. Sound carrier distance is 6.5 MHz. L' is Band I, L is all bands except for Band I
LPL	LG.Philips LCD (supplier)
LS	Loudspeaker
LVDS	Low Voltage Differential Signalling
Mbps	Mega bits per second
M/N	Monochrome TV system. Sound carrier distance is 4.5 MHz
MIPS	Microprocessor without Interlocked Pipeline-Stages; A RISC-based microprocessor
MOP	Matrix Output Processor
MOSFET	Metal Oxide Silicon Field Effect Transistor, switching device
MPEG	Motion Pictures Experts Group
MPIF	Multi Platform InterFace
MUTE	MUTE Line
NC	Not Connected
NICAM	Near Instantaneous Compounded Audio Multiplexing. This is a digital sound system, mainly used in Europe.
NTC	Negative Temperature Coefficient, non-linear resistor
NTSC	National Television Standard Committee. Color system mainly used in North America and Japan. Color carrier NTSC M/N= 3.579545 MHz, NTSC 4.43= 4.433619 MHz (this is a VCR norm, it is not transmitted off-air)
NVM	Non-Volatile Memory: IC containing TV related data such as alignments
O/C	Open Circuit
OSD	On Screen Display
OTC	On screen display Teletext and Control; also called Artistic (SAA5800)
P50	Project 50: communication protocol between TV and peripherals
PAL	Phase Alternating Line. Color system mainly used in West Europe (color carrier= 4.433619 MHz) and South America (color carrier PAL M= 3.575612 MHz and PAL N= 3.582056 MHz)
PCB	Printed Circuit Board (same as “PWB”)
PCM	Pulse Code Modulation
PDP	Plasma Display Panel
PFC	Power Factor Corrector (or Pre-conditioner)
PIP	Picture In Picture
PLL	Phase Locked Loop. Used for e.g. FST tuning systems. The customer can give directly the desired frequency
POD	Point Of Deployment: a removable CAM module, implementing the CA system for a host (e.g. a TV-set)
POR	Power On Reset, signal to reset the uP
PTC	Positive Temperature Coefficient, non-linear resistor
PWB	Printed Wiring Board (same as “PCB”)

PWM	Pulse Width Modulation
QRC	Quasi Resonant Converter
QTNR	Quality Temporal Noise Reduction
QVCP	Quality Video Composition Processor
RAM	Random Access Memory
RGB	Red, Green, and Blue. The primary color signals for TV. By mixing levels of R, G, and B, all colors (Y/C) are reproduced.
RC	Remote Control
RC5 / RC6	Signal protocol from the remote control receiver
RESET	RESET signal
ROM	Read Only Memory
RSDS	Reduced Swing Differential Signalling data interface
R-TXT	Red TeleteXT
SAM	Service Alignment Mode
S/C	Short Circuit
SCART	Syndicat des Constructeurs d'Appareils Radiorécepteurs et Téléviseurs
SCL	Serial Clock I^2C
SCL-F	CLock Signal on Fast I^2C bus
SD	Standard Definition
SDA	Serial Data I^2C
SDA-F	DAta Signal on Fast I^2C bus
SDI	Serial Digital Interface, see “ITU-656”
SDRAM	Synchronous DRAM
SECAM	SEequence Couleur Avec Mémoire. Color system mainly used in France and East Europe. Color carriers= 4.406250 MHz and 4.250000 MHz
SIF	Sound Intermediate Frequency
SMPS	Switched Mode Power Supply
SoC	System on Chip
SOG	Sync On Green
SOPS	Self Oscillating Power Supply
SPI	Serial Peripheral Interface bus; a 4-wire synchronous serial data link standard
S/PDIF	Sony Philips Digital InterFace
SRAM	Static RAM
SRP	Service Reference Protocol
SSB	Small Signal Board
STBY	STand-BY
SVGA	800 × 600 (4:3)
SVHS	Super Video Home System
SW	Software
SWAN	Spatial temporal Weighted Averaging Noise reduction
SXGA	1280 × 1024
TFT	Thin Film Transistor
THD	Total Harmonic Distortion
TMDS	Transmission Minimized Differential Signalling
TXT	TeleteXT
TXT-DW	Dual Window with TeleteXT
UI	User Interface
uP	Microprocessor
UXGA	1600 × 1200 (4:3)
V	V-sync to the module
VESA	Video Electronics Standards Association
VGA	640 × 480 (4:3)
VL	Variable Level out: processed audio output toward external amplifier
VSB	Vestigial Side Band; modulation method
WYSIWYR	What You See Is What You Record: record selection that follows main picture and sound
WXGA	1280 × 768 (15:9)
XTAL	Quartz crystal
XGA	1024 × 768 (4:3)
Y	Luminance signal
Y/C	Luminance (Y) and Chrominance (C) signal
YPbPr	Component video. Luminance and scaled color difference signals (B-Y and R-Y)
YUV	Component video

4. Mechanical Instructions

Index of this chapter:

Notes:

- Figures below can deviate slightly from the actual situation, due to the different set executions.

4.1 Cable Dressing and Taping

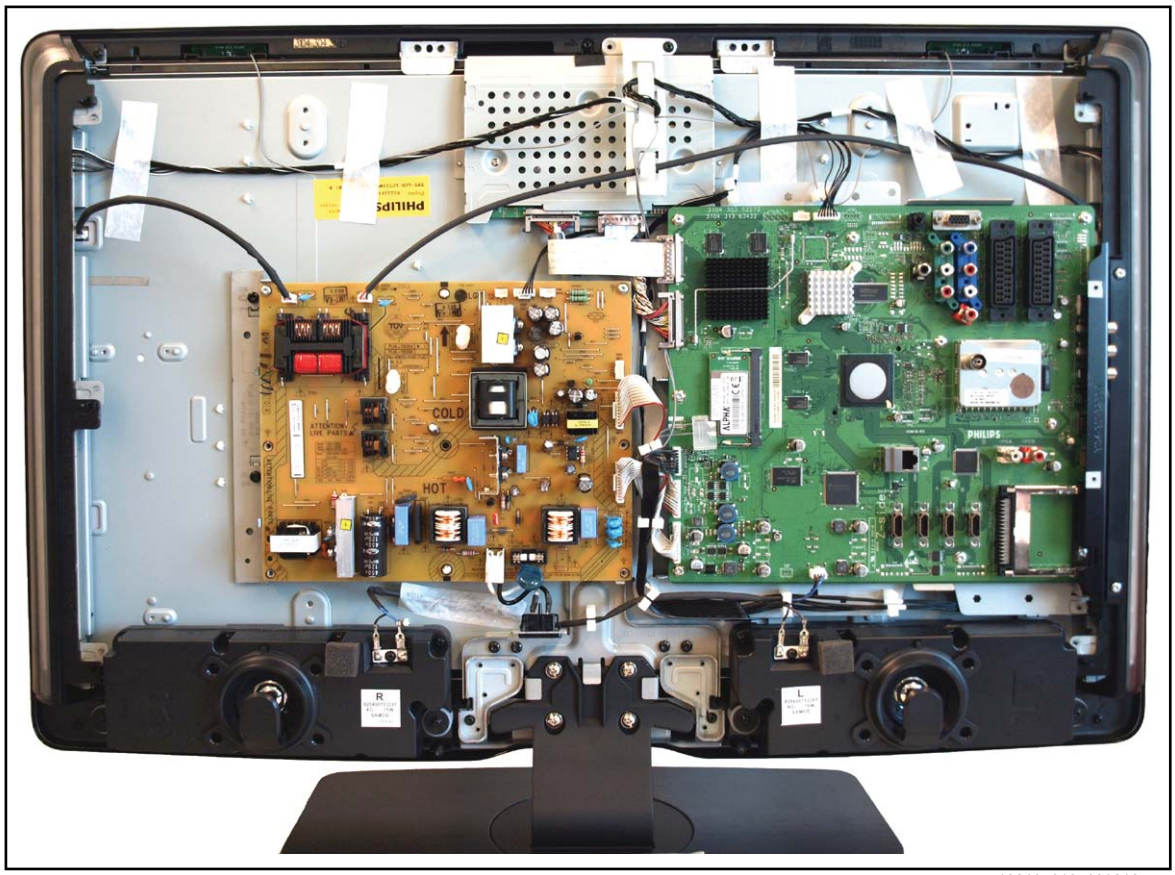

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Figure 4-1 Cable dressing 32”

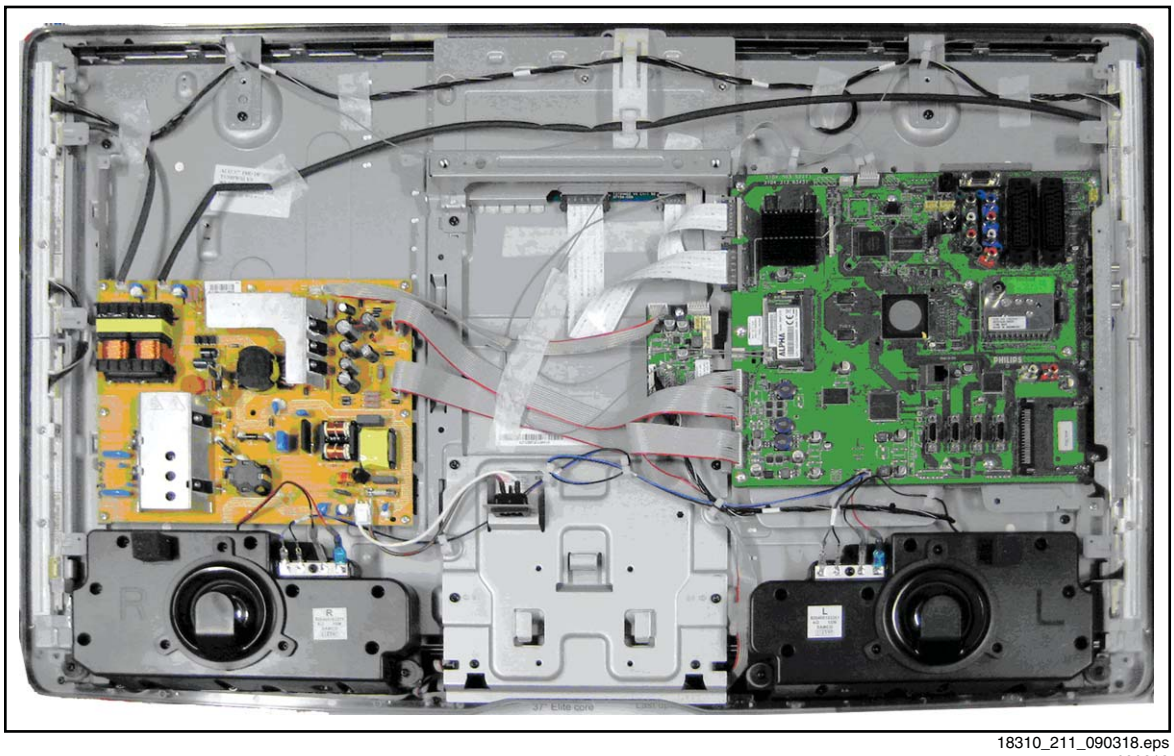

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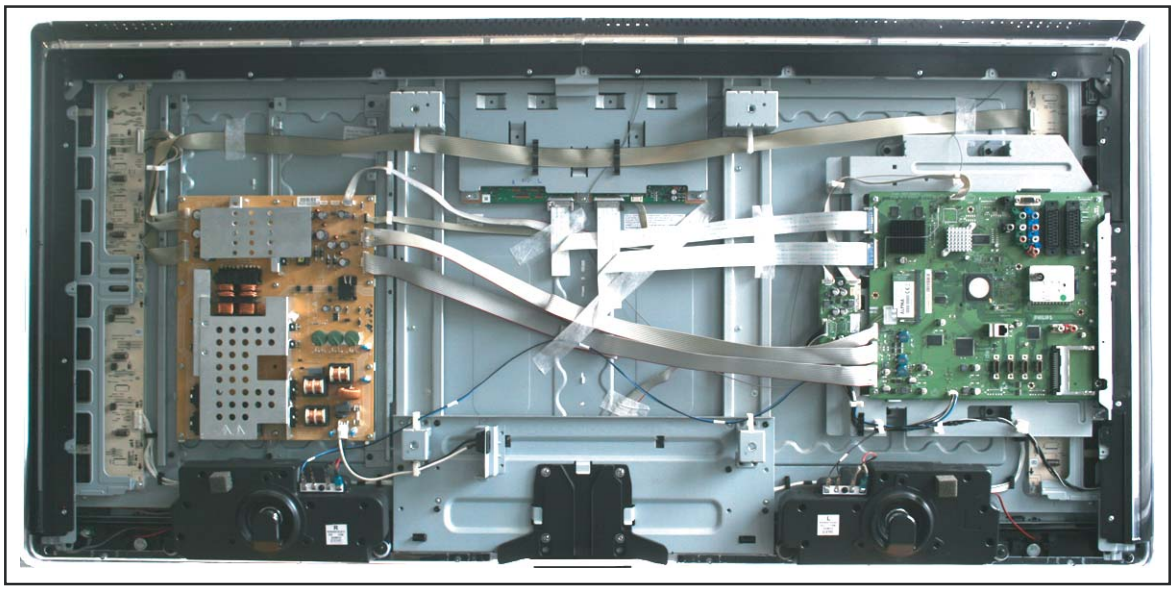
Figure 4-2 Cable dressing 37"



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090506

Figure 4-3 Cable dressing 56" (21:9)

4.2 Service Positions

For easy servicing of this set, there are a few possibilities created:

- The buffers from the packaging.
- Foam bars (created for Service).

4.2.1 Foam Bars

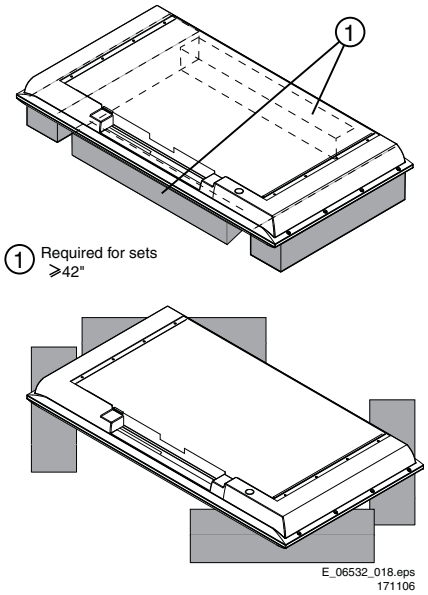


Figure 4-4 Foam bars

The foam bars (order code 3122 785 90580 for two pieces) can be used for all types and sizes of Flat TVs.
See Figure 4-4 for details. Sets with a display of 42" and larger, require **four** foam bars [1]. Ensure that the foam bars are always supporting the cabinet and **never** only the display.
Caution: Failure to follow these guidelines can seriously damage the display!
By laying the TV face down on the (ESD protective) foam bars, a stable situation is created to perform measurements and alignments. By placing a mirror under the TV, you can monitor the screen.

4.3 Assy/Panel Removal

4.3.1 Rear Cover

Warning: Disconnect the mains power cord before you remove the rear cover.
Note: it is **not** necessary to remove the stand while removing the rear cover.

Removing the Piezo Touch Control Panel PWB requires special attention. Refer to Piezo Touch Control Panel ***for details.***

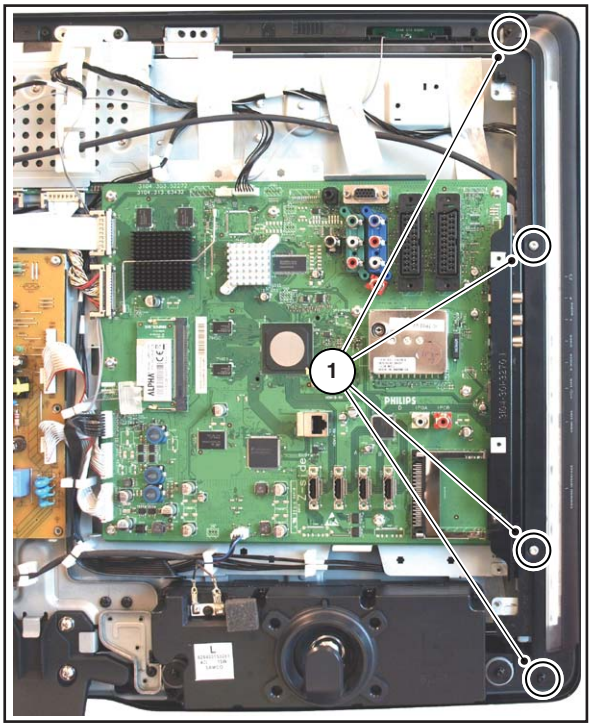
1. Remove all screws of the rear cover.
2. Lift the rear cover from the TV. Make sure that wires and flat coils are not damaged while lifting the rear cover from the set.

4.3.2 Speakers

Each speaker unit is mounted with two screws. A sticker on the the unit indicates if it is the right (“R”) or left (“L”) box, seen from the front side of the set.
When defective, replace the whole unit.

4.3.3 Ambi Light

Each Ambi Light unit is mounted on a subframe. Refer to Figure 4-5 for details.



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090319

Figure 4-5 Ambi Light unit

1. Remove the Ambi Light cover [1].
2. Unplug the connector(s).
3. The PWB can now be taken from the subframe.

When defective, replace the whole unit.
Note: the screws that secure the AmbiLight units are longer than the other screws.

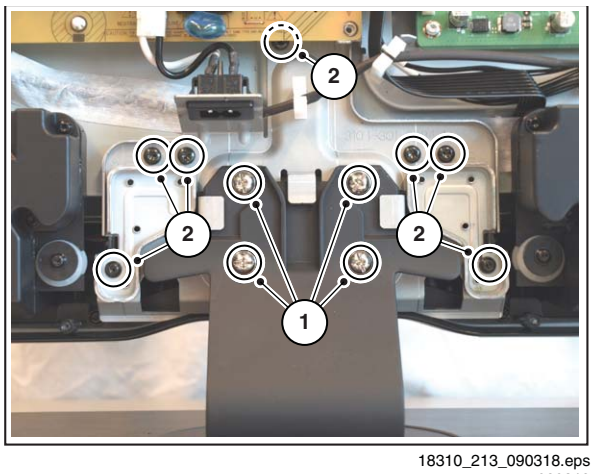
4.3.4 Main Supply Panel

1. Unplug all connectors.
2. Remove the fixation screws.
3. Take the board out.

When defective, replace the whole unit.

4.3.5 IR & LED Board

Refer to Figure 4-6 for details.



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090319

Figure 4-6 IR & LED Board

1. Remove the Main Supply Panel as earlier described.
2. Remove the stand [1] and its subframe [2].
3. Now you gain access the IR & LED board.

When defective, replace the whole unit.

4.3.6 Piezo Touch Control Panel

The flexfoil between Piezo Flexfoil Assy (mounted on the plastic rim of the set), and the PWB as described below, is extremely vulnerable. Do not pull hard at the PWB or flexfoil.
Once the flexfoil has been damaged, the entire plastic rim of the set (with the touch-control pads) has to be swapped!

The Piezo Touch Control Panel PWB contains ESD sensitive components, implying that necessary industrial ESD precautions must be taken during removing or remounting. Refer to Figure 4-7, Figure 4-8 and Figure 4-9 for details.

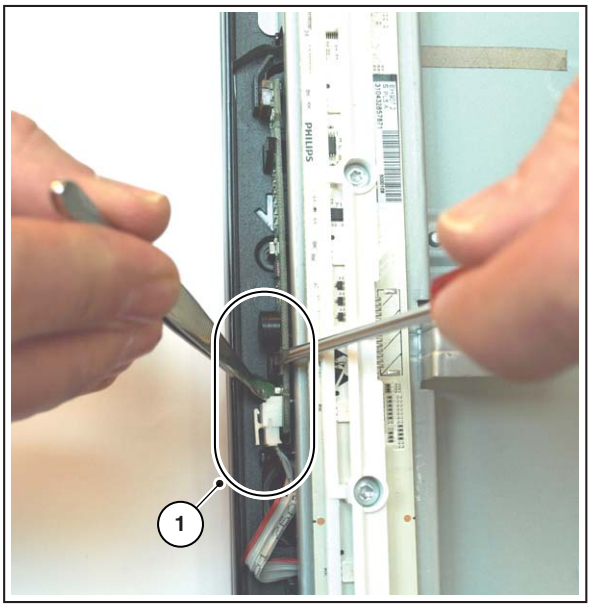

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Figure 4-7 Piezo Touch Control Panel -1-

1. Gently pull the bottom side of the PWB out of the cabinet until you can unplug the connector [1].

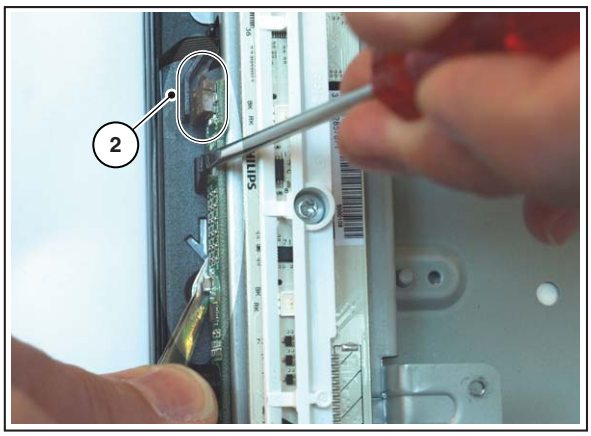

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Figure 4-8 Piezo Touch Control Panel -2-

1. Now gently pull the top side of the PWB out of the cabinet **without damaging the flexfoil** until you can unplug the connector [2].

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090319

Figure 4-9 Piezo Touch Control Panel -3-

1. To unplug the flexfoil connector, first the outer part of the connector has to be moved upwards [3], before this part can be turned sidewards [4] as shown in the picture. Now the flexfoil can be removed from the connector and the PWB can be taken out of the set.

When defective, replace the whole unit.

4.3.7 Small Signal Board (SSB)

Caution: It is mandatory to remount screws at their original position during re-assembly. Failure to do so may result in damaging the SSB.

1. Remove the Wi-Fi module that is mounted on the SSB.
2. Unplug all connectors.
3. Remove the screws that secure the board.
4. The SSB can now be taken out of the set.

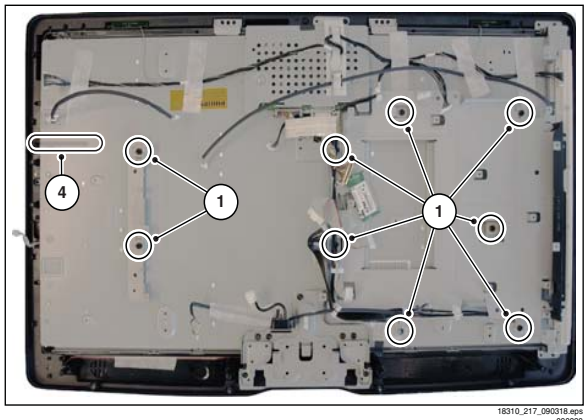
4.3.8 LCD Panel

Refer to Figure 4-10 and Figure 4-11 for details.

1. Remove the Piezo Touch Control Panel PWB as earlier described.
2. Remove the AL covers as earlier described.
3. Remove both Main Supply Panel and SSB as earlier described.
4. Remove the subframes of Main Power Supply and SSB [1].
5. Remove both AL subframes (with the AL unit still mounted on it) by unplugging the connector [2] and removing the screws [3].
6. Remove all remaining adhesive tapes and remove all cables from their clamps.
7. Carefully remove the conducting tape [4], it must be re-used during re-assembly!
8. Remove the remaining screws (indicated with an arrow) that hold the plastic rim and remove the rim.
9. Now the LCD Panel can be lifted from the front cabinet. **The panel has to be slided downwards** once it has been lifted, because the brackets on the top cannot be removed from the cabinet. You will see a conducting foam between metal front and panel, near the location of the Piezo Touch Control Panel.

When mounting a new LCD Panel:

1. Check if this conducting foam between panel and metal front is in place !
2. Re-attach the conducting tape between LCD Panel and metal rim [4] !



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090320

Figure 4-10 LCD Panel -1-

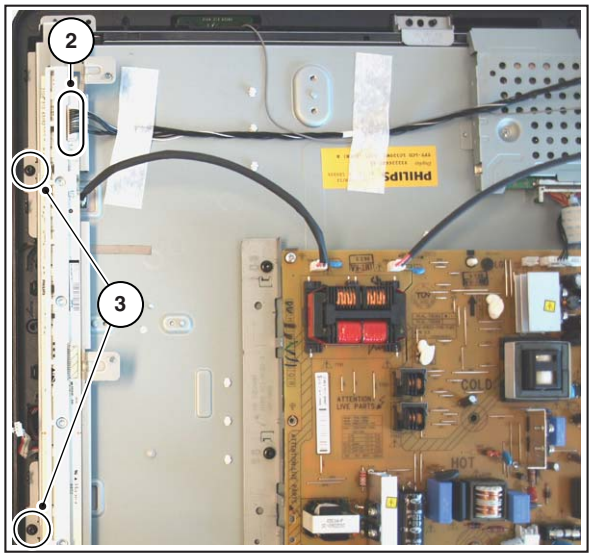

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Figure 4-11 LCD Panel -2-

4.3.9 Wi-Fi antenna

Follow the instructions for LCD Panel until “remove plastic rim”. After removal of this rim, you gain access to the Wi-Fi antennas.

4.4 Set Re-assembly

To re-assemble the whole set, execute all processes in reverse order.

Notes:

- While re-assembling, make sure that all cables are placed and connected in their original position.
- Pay special attention not to damage the EMC foams in the set. Ensure that EMC foams are mounted correctly.

5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

5.1 Test Points

As most signals are digital, it will be difficult to measure waveforms with a standard oscilloscope. However, several key ICs are capable of generating test patterns, which can be controlled via ComPair. In this way it is possible to determine which part is defective.

Perform measurements under the following conditions:
- Service Default Mode.
- Video: Colour bar signal.
- Audio: 3 kHz left, 1 kHz right.

5.2 Service Modes

Service Default mode (SDM) and Service Alignment Mode (SAM) offers several features for the service technician, while the Customer Service Mode (CSM) is used for communication between the call centre and the customer.

This chassis also offers the option of using ComPair, a hardware interface between a computer and the TV chassis. It offers the abilities of structured troubleshooting, error code reading, and software version read-out for all chassis. (see also section “5.4.1 ComPair”).

Note: For the new model range, a new remote control (RC) is used with some renamed buttons. This has an impact on the activation of the Service modes. For instance the old “MENU” button is now called “HOME” (or is indicated by a “house” icon).

5.2.1 Service Default Mode (SDM)

Purpose
- To create a pre-defined setting, to get the same measurement results as given in this manual.
- To override SW protections detected by stand-by processor and make the TV start up to the step just before protection (a sort of automatic stepwise start-up). See section “5.3 Stepwise Start-up”.
- To start the blinking LED procedure where only LAYER 2 errors are displayed. (see also section “5.5 Error Codes”).

Specifications

Table 5-1 SDM default settings

Region	Freq. (MHz)	Default system
Europe, AP(PAL/Multi)	475.25	PAL B/G
Europe, AP DVB-T	546.00 PID Video: 0B 06 PID PCR: 0B 06 PID Audio: 0B 07	DVB-T

- All picture settings at 50% (brightness, colour, contrast).
- All sound settings at 50%, except volume at 25%.
- All service-unfriendly modes (if present) are disabled, like:
  - (Sleep) timer.
  - Child/parental lock.
  - Picture mute (blue mute or black mute).
  - Automatic volume levelling (AVL).
  - Skip/blank of non-favourite pre-sets.

How to Activate SDM

For this chassis there are two kinds of SDM: an **analog SDM** and a **digital SDM**. Tuning will happen according Table 5-1.
- **Analog SDM**: use the standard RC-transmitter and key in the code “062596”, directly followed by the “MENU” (or HOME) button.
  Note: It is possible that, together with the SDM, the main menu will appear. To switch it “off”, push the “MENU”(or HOME) button again.
- **Digital SDM**: use the standard RC-transmitter and key in the code “062593”, directly followed by the “MENU” (or HOME) button.
  Note: It is possible that, together with the SDM, the main menu will appear. To switch it “off”, push the “MENU” (or HOME) button again.
- **Analog SDM** can also be activated by grounding for a moment the solder pad on the SSB, with the indication “SDM” (see Service mode pad).

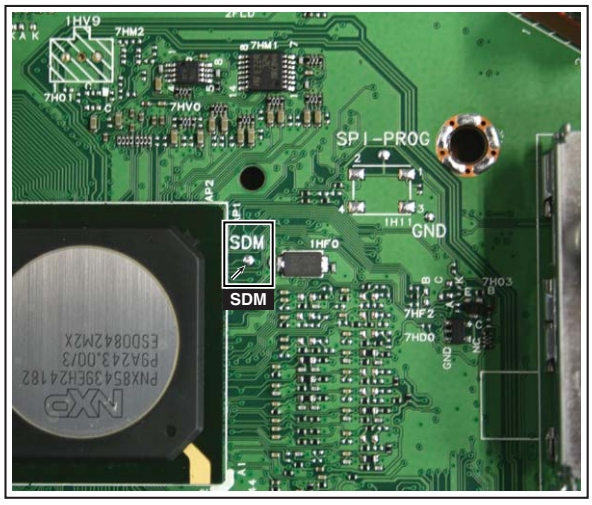

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Figure 5-1 Service mode pad

After activating this mode, “SDM” will appear in the upper right corner of the screen (when a picture is available).

How to Navigate
When the “MENU” (or HOME) button is pressed on the RC transmitter, the TV set will toggle between the SDM and the normal user menu.

How to Exit SDM
Use one of the following methods:
- Switch the set to STAND-BY via the RC-transmitter.
- Via a standard customer RC-transmitter: key in “00”-sequence.

5.2.2 Service Alignment Mode (SAM)

Purpose
- To perform (software) alignments.
- To change option settings.
- To easily identify the used software version.

- To view operation hours.
- To display (or clear) the error code buffer.

How to Activate SAM

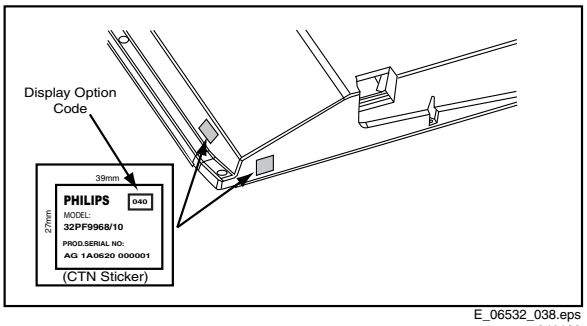
Via a standard RC transmitter: Key in the code “062596” directly followed by the “INFO” button. After activating SAM with this method a service warning will appear on the screen, continue by pressing the “OK” button on the RC.

Contents of SAM (see also Table 6-4)

- **Hardware Info.**
  - **A. SW Version.** Displays the software version of the main software (**example:** Q5492-1.2.3.4 = AAAAB_X.Y.W.Z).
    - **AAAA**= the chassis name.
    - **B**= the SW branch version. This is a sequential number (this is no longer the region indication, as the software is now multi-region).
    - **X.Y.W.Z**= the software version, where X is the main version number (different numbers are not compatible with one another) and Y.W.Z is the sub version number (a higher number is always compatible with a lower number).
  - **B. STBY PROC Version.** Displays the software version of the stand-by processor.
  - **C. Production Code**. Displays the production code of the TV, this is the serial number as printed on the back of the TV set. Note that if an NVM is replaced or is initialized after corruption, this production code has to be re-written to NVM. ComPair will foresee in a possibility to do this.
- **Operation Hours.** Displays the accumulated total of operation hours (not the stand-by hours). Every time the TV is switched “on/off”, 0.5 hours is added to this number.
- **Errors** (followed by maximum 10 errors). The most recent error is displayed at the upper left (for an error explanation see section “5.5 Error Codes”).
- **Reset Error Buffer.** When “cursor right” (or the “OK button) is pressed and then the “OK” button is pressed, the error buffer is reset.
- **Alignments.** This will activate the “ALIGNMENTS” sub-menu. See Chapter 6. Alignments.
- **Dealer Options.** Extra features for the dealers.
- **Options.** Extra features for Service. For more info regarding option codes, 6. Alignments.
  Note that if the option code numbers are changed, these have to be confirmed with pressing the “OK” button before the options are stored. Otherwise changes will be lost.
- **Initialize NVM.** The moment the processor recognizes a corrupted NVM, the “initialize NVM” line will be highlighted. Now, two things can be done (dependent of the service instructions at that moment):
  - Save the content of the NVM via ComPair for development analysis, **before** initializing. This will give the Service department an extra possibility for diagnosis (e.g. when Development asks for this).
  - Initialize the NVM.

Note: When the NVM is corrupted, or replaced, there is a high possibility that no picture appears because the display code is not correct. So, before initializing the NVM via the SAM, a picture is necessary and therefore the correct display option has to be entered. Refer to Chapter 6. Alignments for details. To adapt this option, it’s advised to use ComPair (the correct HEX values for the options can be found in Chapter 6. Alignments) or a method via a standard RC (described below).

Changing the display option via a standard RC: Key in the code “062598” directly followed by the “MENU” (or HOME) button and “XXX” (where XXX is the 3 digit decimal display code as mentioned in Table 6-3). Make sure to key in all three digits, also the leading zero’s. If the above action is successful, the front LED will go out as an indication that the RC sequence was correct. After the display option is changed in the NVM, the TV will go to the Stand-by mode. If the NVM was corrupted or empty before this action, it will be initialized first (loaded with default values). This initializing can take up to 20 seconds.



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240108

Figure 5-2 Location of Display Option Code sticker

- **Store - go right.** All options and alignments are stored when pressing “cursor right” (or the “OK” button) and then the “OK”-button.
- **SW Maintenance.**
  - **SW Events.** Not useful for Service purposes. In case of specific software problems, the development department can ask for this info.
  - **HW Events.** Not useful for Service purposes. In case of specific software problems, the development department can ask for this info.
- **Operation hours display.** Displays the accumulated total of display operation hours. So, this one keeps up the lifetime of the display itself, mainly to compensate the degeneration behaviour.
- **Test settings.** For development purposes only.
- **Development file versions.** Not useful for Service purposes, this information is only used by the development department.
- **Upload to USB.** To upload several settings from the TV to an USB stick, which is connected to the SSB. The items are “Channel list”, “Personal settings”, “Option codes”, “Display-related alignments” and “History list”. **First a directory “repair\” has to be created in the root of the USB stick.** To upload the settings select each item separately, press “cursor right” (or the “OK” button), confirm with “OK” and wait until “Done” appears. In case the download to the USB stick was not successful “Failure” will appear. In this case, check if the USB stick is connected properly and if the directory “repair” is present in the root of the USB stick. Now the settings are stored onto the USB stick and can be used to download onto another TV or other SSB. Uploading is of course only possible if the software is running and if a picture is available. This method is created to be able to save the customer’s TV settings and to store them into another SSB.
- **Download to USB.** To download several settings from the USB stick to the TV, same way of working needs to be followed as with uploading. To make sure that the download of the channel list from USB to the TV is executed properly, it is necessary to restart the TV and tune to a valid preset if necessary.
  Note: The “History list item” can not be downloaded from USB to the TV. This is a “read-only” item. In case of specific problems, the development department can ask for this info.

How to Navigate

- In SAM, the menu items can be selected with the “CURSOR UP/DOWN” key on the RC-transmitter. The selected item will be highlighted. When not all menu items fit on the screen, move the “CURSOR UP/DOWN” key to display the next/previous menu items.
- With the “CURSOR LEFT/RIGHT” keys, it is possible to:
  - (De) activate the selected menu item.
  - (De) activate the selected sub menu.

- With the “OK” key, it is possible to activate the selected action.

How to Exit SAM

Use one of the following methods:

- Switch the TV set to STAND-BY via the RC-transmitter.
- Via a standard RC-transmitter, key in “00” sequence, or select the “BACK” key.

5.2.3 Customer Service Mode (CSM)

Purpose

When a customer is having problems with his TV-set, he can call his dealer or the Customer Helpdesk. The service technician can then ask the customer to activate the CSM, in order to identify the status of the set. Now, the service technician can judge the severity of the complaint. In many cases, he can advise the customer how to solve the problem, or he can decide if it is necessary to visit the customer.
The CSM is a read only mode; therefore, modifications in this mode are not possible.
When in this chassis CSM is activated, a testpattern will be displayed during 5 seconds (1 second Blue, 1 second Green and 1 second Red, then again 1 second Blue and 1 second Green). This test pattern is generated by the PNX5100. So if this test pattern is shown, it could be determined that the back end video chain (PNX5100, LVDS, and display) of the SSB is working.
When CSM is activated and there is a USB stick connected to the TV, the software will dump the complete CSM content to the USB stick. The file (Csm.txt) will be saved in the root of the USB stick. This info can be handy if no information is displayed.

Also when CSM is activated, the LAYER 1 error is displayed via blinking LED. Only the latest error is displayed. (see also section 5.5 Error Codes).

How to Activate CSM

Key in the code “123654” via the standard RC transmitter.

Note: Activation of the CSM is only possible if there is no (user) menu on the screen!

How to Navigate

By means of the “CURSOR-DOWN/UP” knob on the RC-transmitter, can be navigated through the menus.

Contents of CSM

The contents are reduced to 3 pages: General, Software versions and Quality items. The group names itself are not shown anywhere in the CSM menu.

General

- **Set Type.** This information is very helpful for a helpdesk/ workshop as reference for further diagnosis. In this way, it is not necessary for the customer to look at the rear of the TV-set. Note that if an NVM is replaced or is initialized after corruption, this set type has to be re-written to NVM. ComPair will foresee in a possibility to do this.
- **Production Code.** Displays the production code (the serial number) of the TV. Note that if an NVM is replaced or is initialized after corruption, this production code has to be re-written to NVM. ComPair will foresee a in possibility to do this.
- **Installed date.** Indicates the date of the first installation of the TV. This date is acquired via time extraction.
- **Options 1.** Gives the option codes of option group 1 as set in SAM (Service Alignment Mode).
- **Options 2.** Gives the option codes of option group 2 as set in SAM (Service Alignment Mode).
- **12NC SSB.** Gives an identification of the SSB as stored in NVM. Note that if an NVM is replaced or is initialized after corruption, this identification number has to be re-written to NVM. ComPair will foresee in a possibility to do this. This identification number is the 12nc number of the SSB.
- **12NC display.** Shows the 12NC of the display.
- **12NC supply.** Shows the 12NC of the supply.
- **12NC “fan board”.** Shows the 12NC of the “fan board”-module (for sets with LED backlight)
- **12NC “LED Dimming Panel”.** Shows the 12NC of the LED dimming Panel (for sets with LED backlight).

Software versions

- **Current main SW.** Displays the built-in main software version. In case of field problems related to software, software can be upgraded. As this software is consumer upgradeable, it will also be published on the Internet.
  Example: Q5492_1.2.3.4
- **Standby SW.** Displays the built-in stand-by processor software version. Upgrading this software will be possible via ComPair or via USB (see section 5.9 Software Upgrading).
  Example: STDBY_88.68.1.2.
- **MOP ambient light SW.** Displays the MOP ambient light EPLD SW.
- **LED Dimming SW.** Displays the LED Dimming EPLD SW-version (for sets with LED backlight).
- **Local contrast SW.** Displays the MOP local contrast SW-version.

Quality items

- **Signal quality.** Poor / average /good
- **Child lock.** Not active / active. This is a combined item for locks. If any lock (Preset lock, child lock, lock after or parental lock) is active, the item shall show “active”.
- **HDMI HDCP key.** Indicates if the HDMI keys (or HDCP keys) are valid or not. In case these keys are not valid and the customer wants to make use of the HDMI functionality, the SSB has to be replaced.
- **Ethernet MAC address.** Displays the MAC address present in the SSB.
- **Wireless MAC address.** Displays the wireless MAC address to support the Wi-Fi functionality.
- **BDS key.** Indicates if the “BDS level 1” key is valid or not.
- **CI slot present.** If the common interface module is detected the result will be “YES” or “NO”.
- **HDMI input format.** The detected input format of the HDMI.
- **HDMI audio input stream.** The HDMI audio input stream is displayed: present / not present.
- **HDMI video input stream.** The HDMI video input stream is displayed: present / not present.

How to Exit CSM

Press “MENU” (or HOME) / “Back” key on the RC-transmitter.

5.3 Stepwise Start-up

When the TV is in a protection state due to an error detected by stand-by software (error blinking is displayed) **and** SDM is activated via shortcutting the pins on the SSB, the TV starts up until it reaches the situation just before protection. So, this is a kind of automatic stepwise start-up. In combination with the start-up diagrams below, you can see which supplies are present at a certain moment. Important to know is, that if e.g. the 3V3 detection fails and thus error layer 2 = 18 is blinking while the TV is restarted via SDM, the Stand-by Processor will enable the 3V3, but the TV set will not go to protection now. The TV will stay in this situation until it is reset (Mains/AC Power supply interrupted). **Caution:** in case the start-up in this mode with a faulty FET 7U08 is done, you can destroy all IC's supplied by the +3V3, due to overvoltage (12V on 3V3-line). It is recommended to measure first the FET 7U08 or others FET's on shortcircuit before activating SDM via the service pads.

The abbreviations "SP" and "MP" in the figures stand for:

- SP: protection or error detected by the **S**tand-by **P**rocessor.
- MP: protection or error detected by the MIPS **M**ain **P**rocessor.

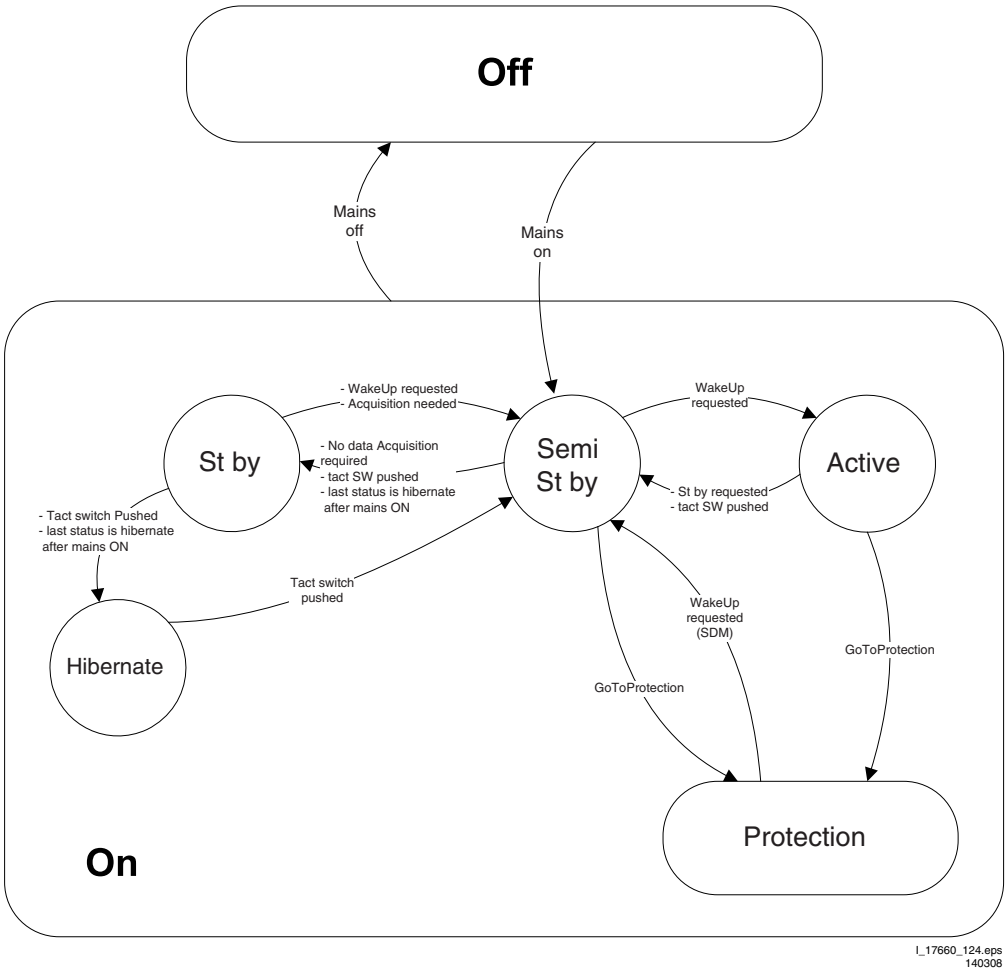


Figure 5-3 Transition diagram

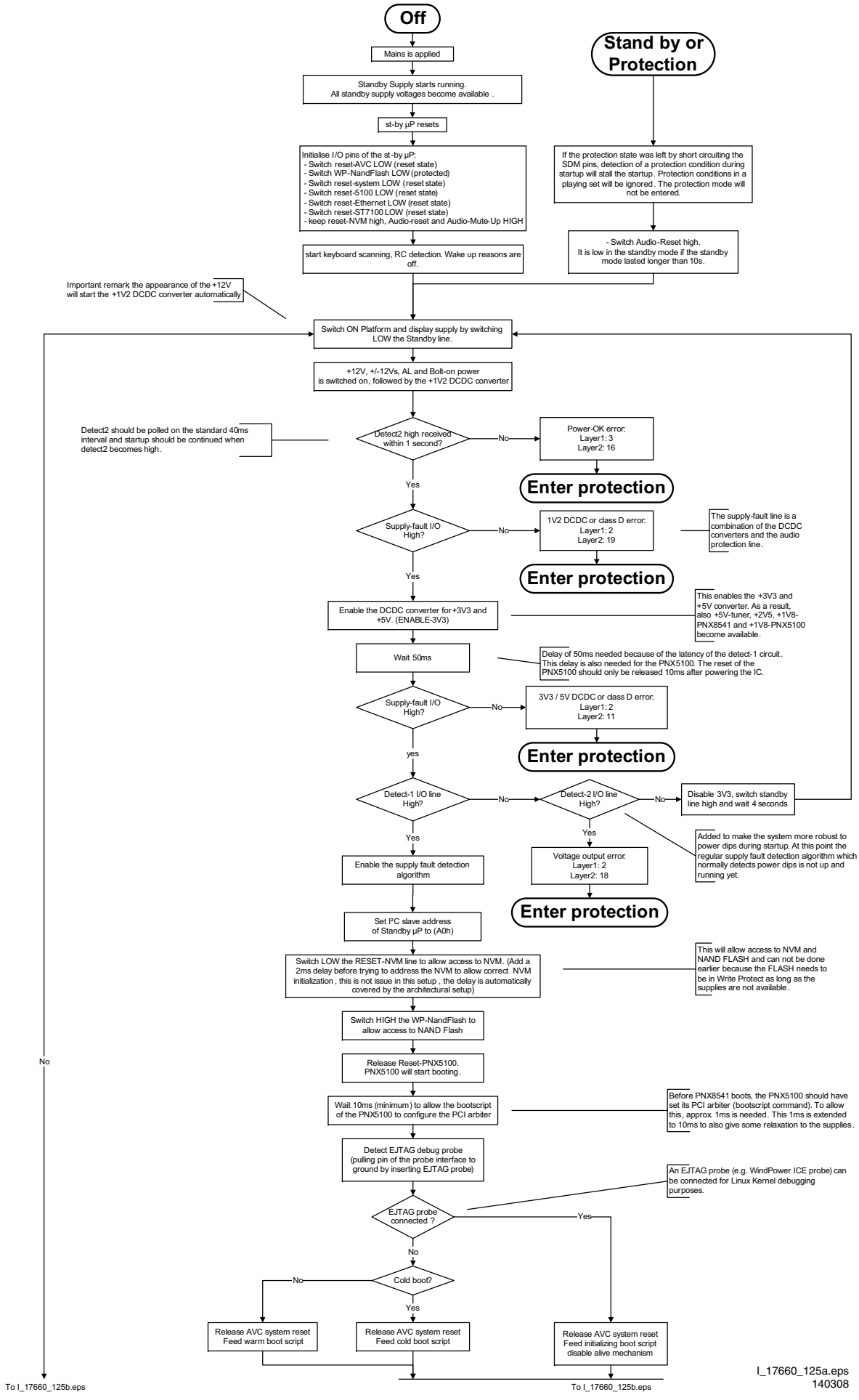


Figure 5-4 "Off" to "Semi Stand-by" flowchart (part 1)

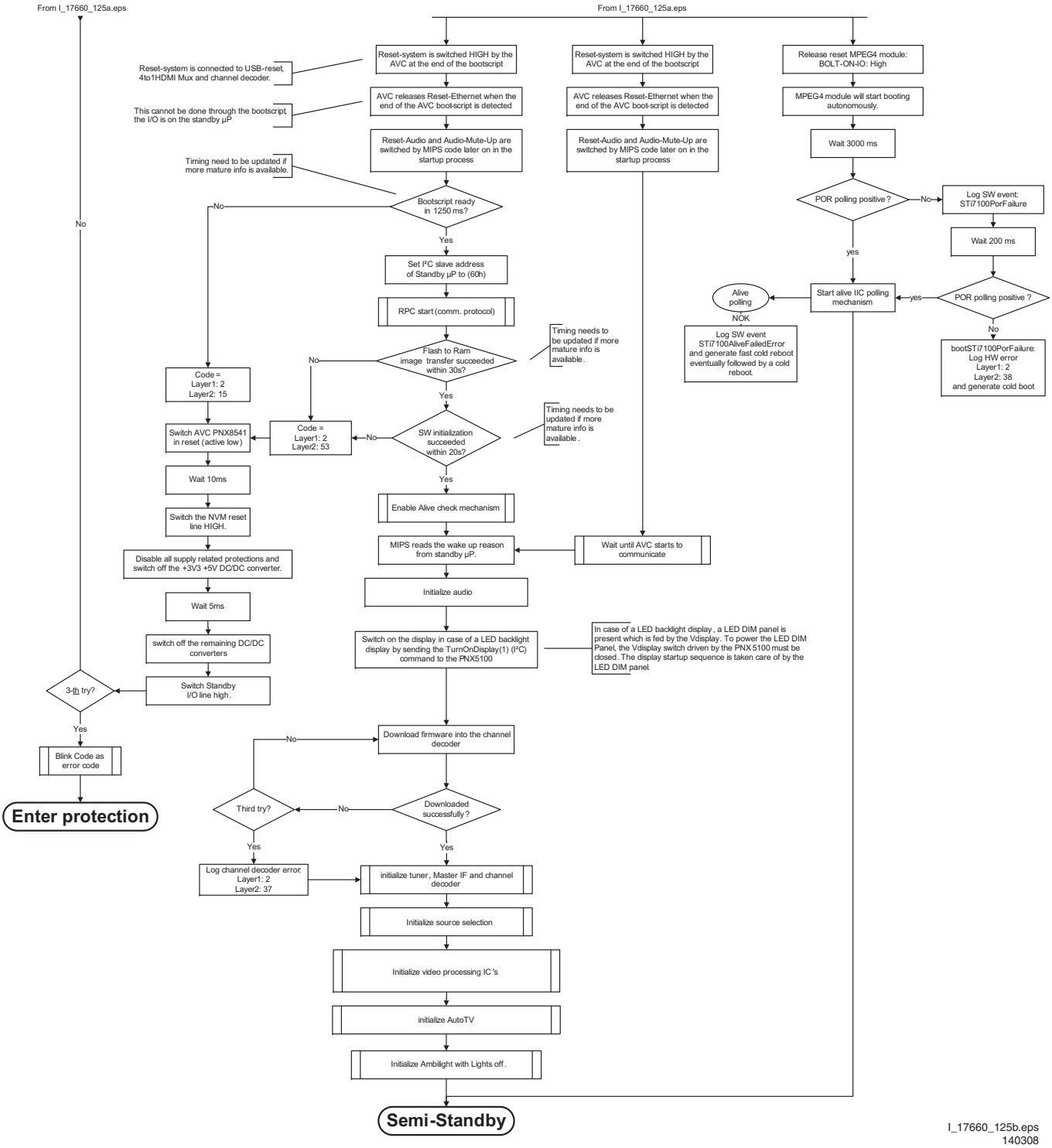


Figure 5-5 "Off" to "Semi Stand-by" flowchart (part 2)

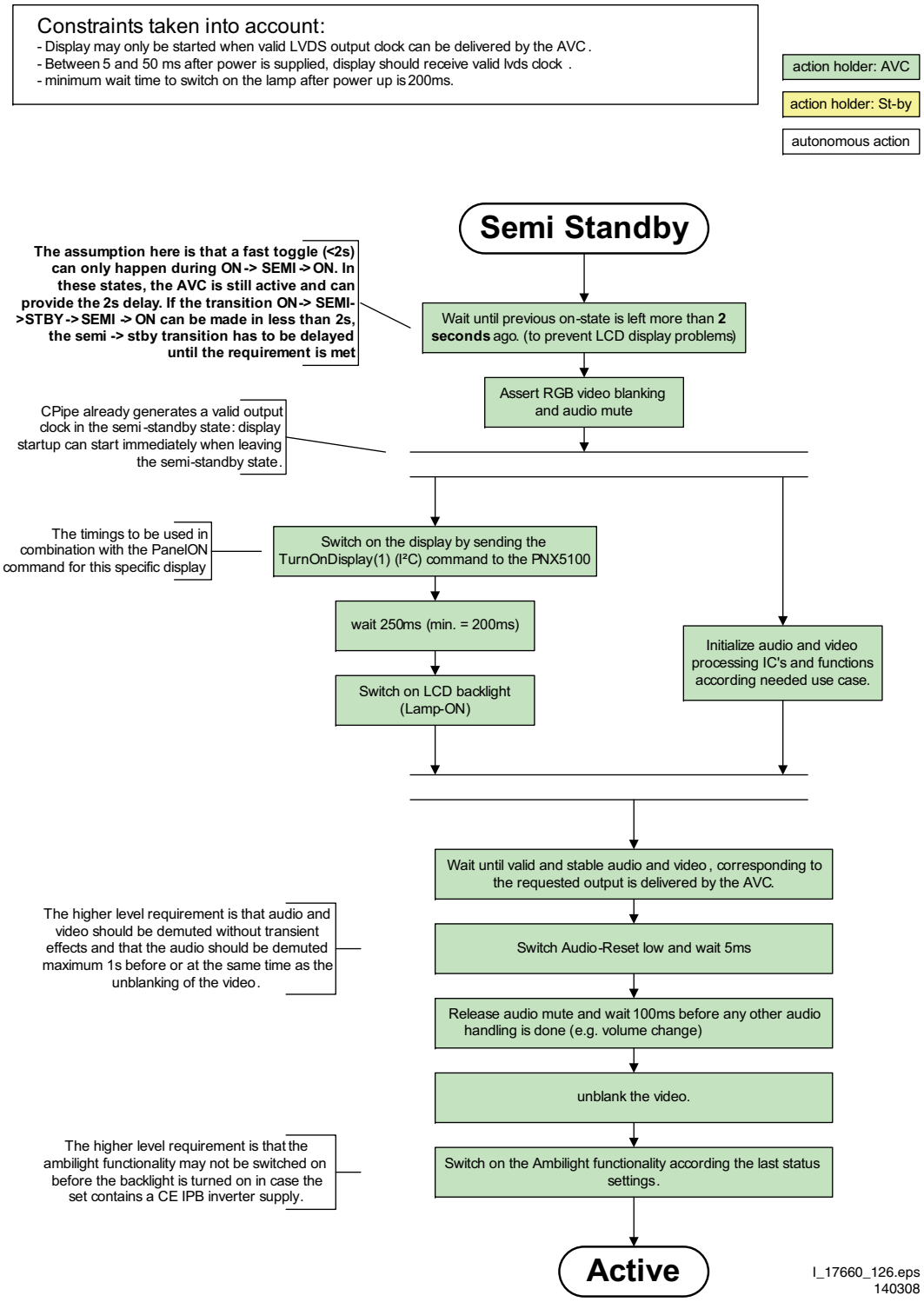


Figure 5-6 "Semi Stand-by" to "Active" flowchart

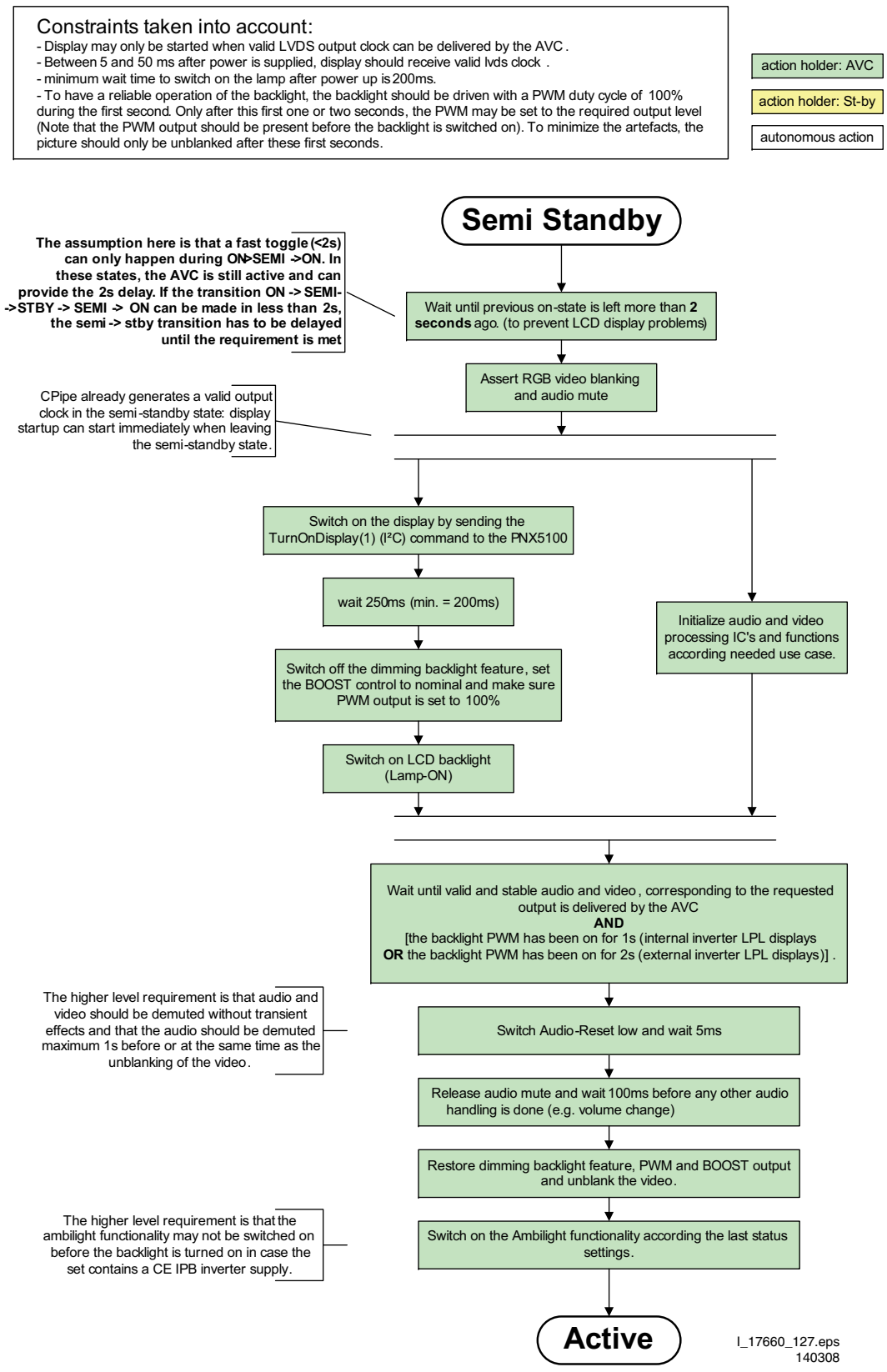


Figure 5-7 "Semi Stand-by" to "Active" flowchart LCD with preheat

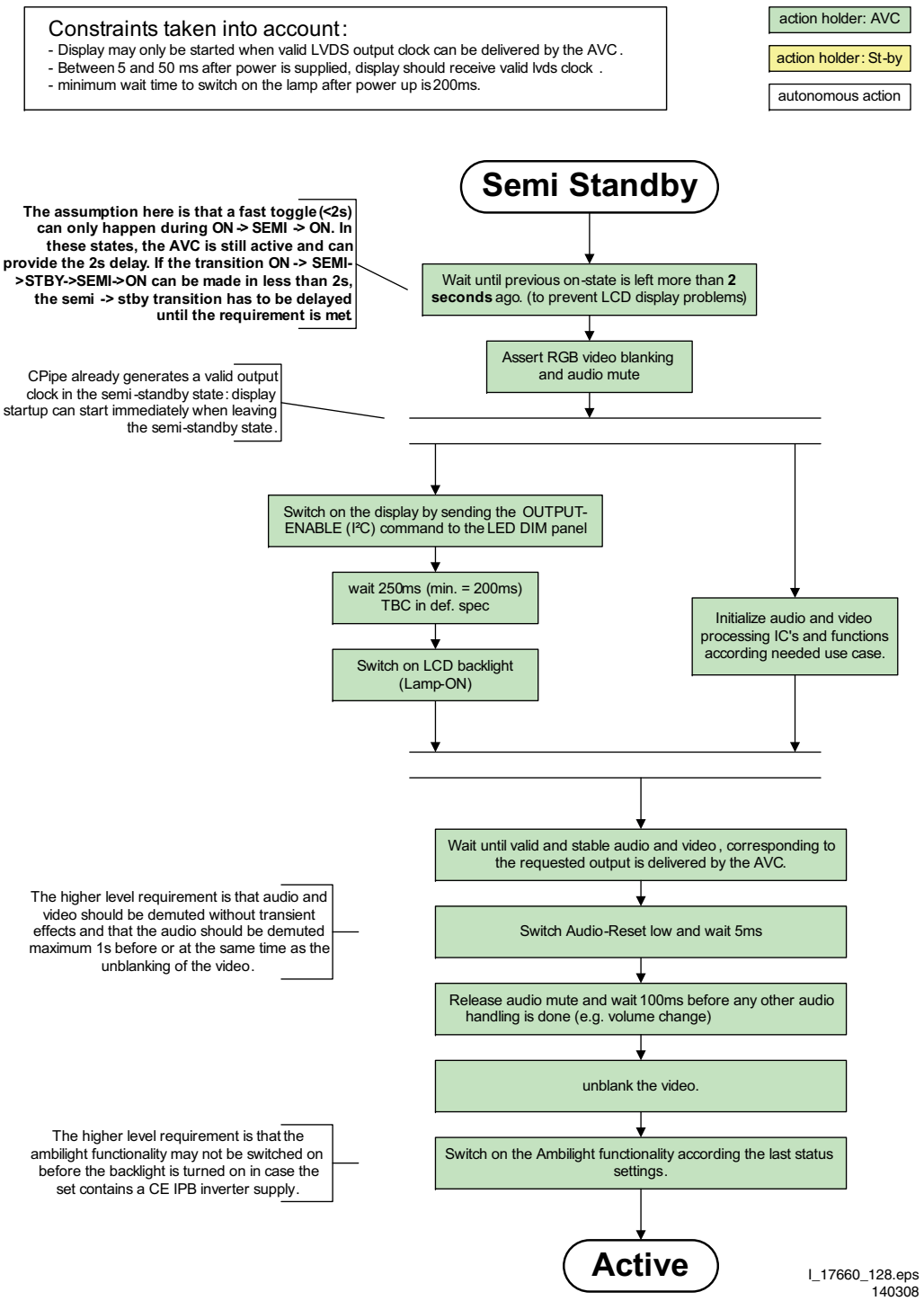


Figure 5-8 "Semi Stand-by" to "Active" flowchart (LED backlight)

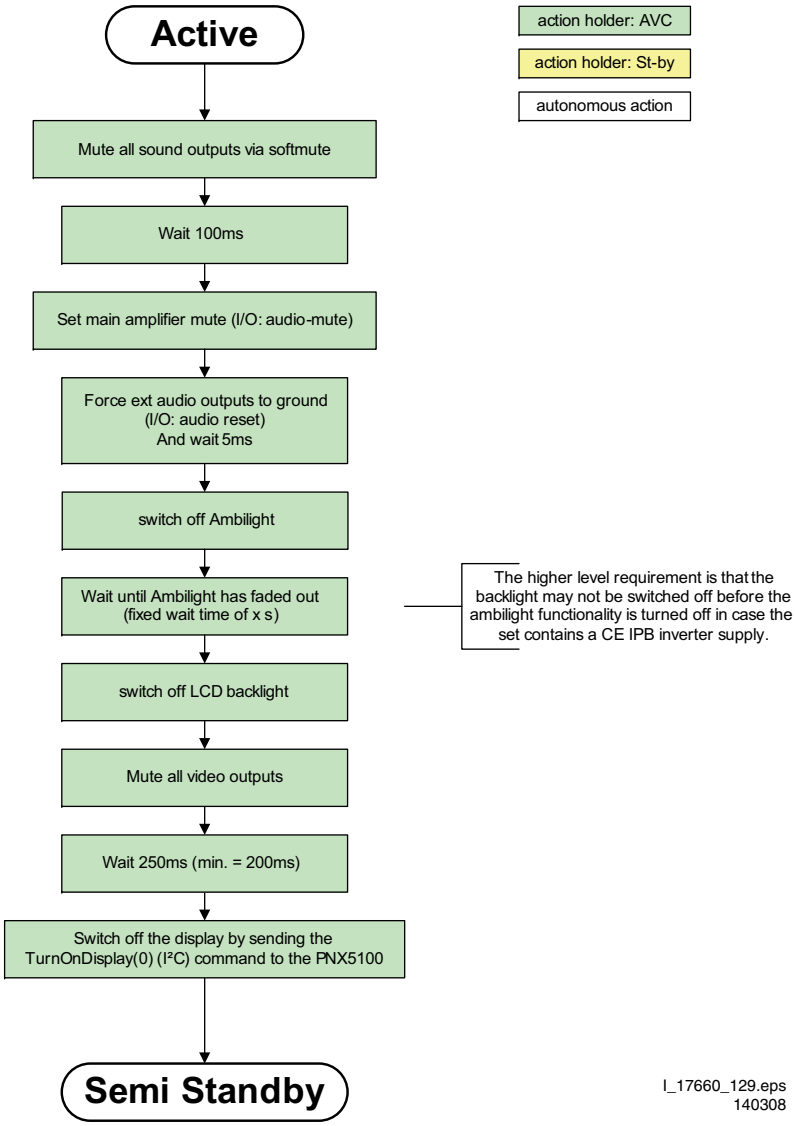


Figure 5-9 “Active” to “Semi Stand-by” flowchart (LCD non DFI)

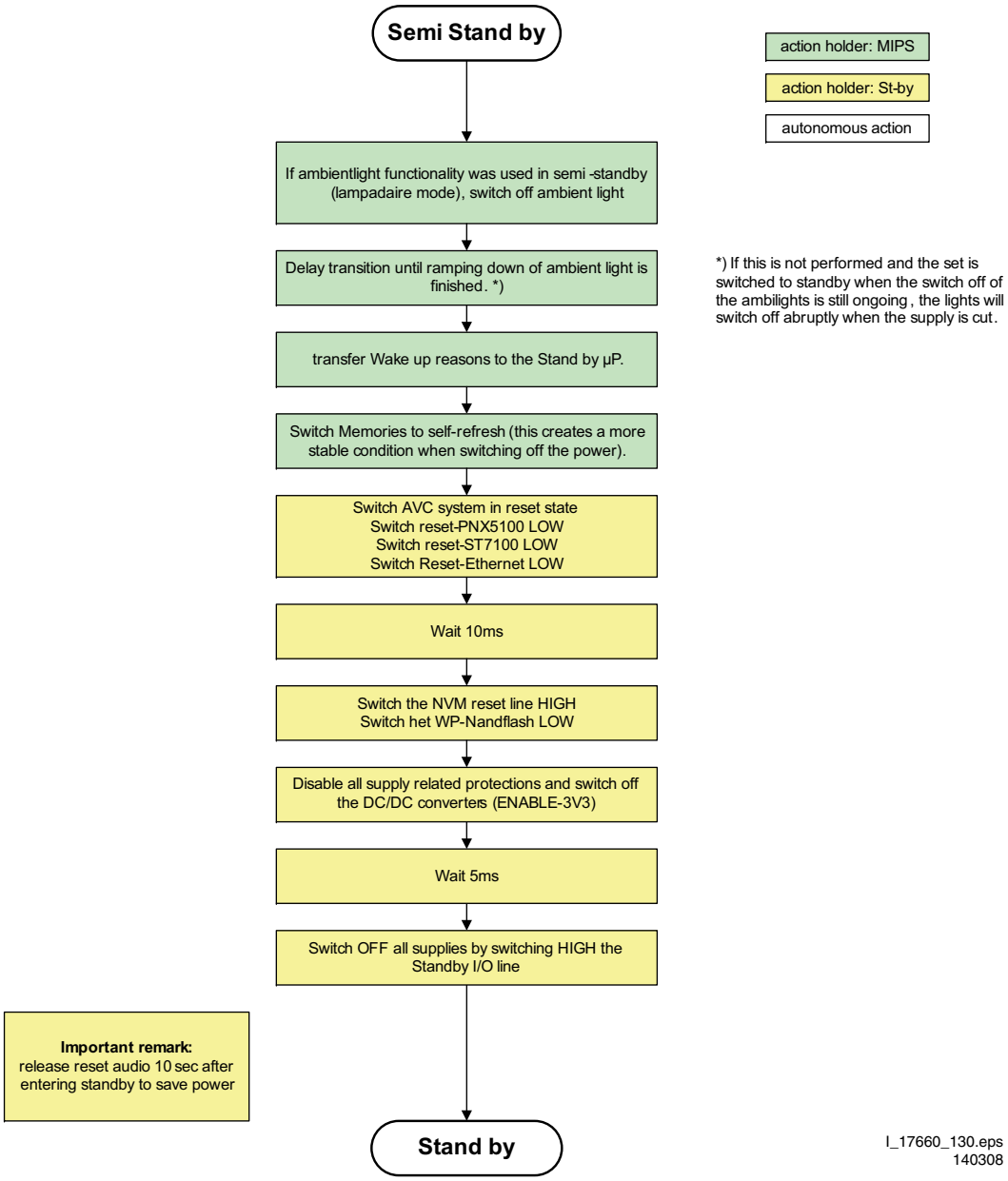


Figure 5-10 "Semi Stand-by" to "Stand-by" flowchart

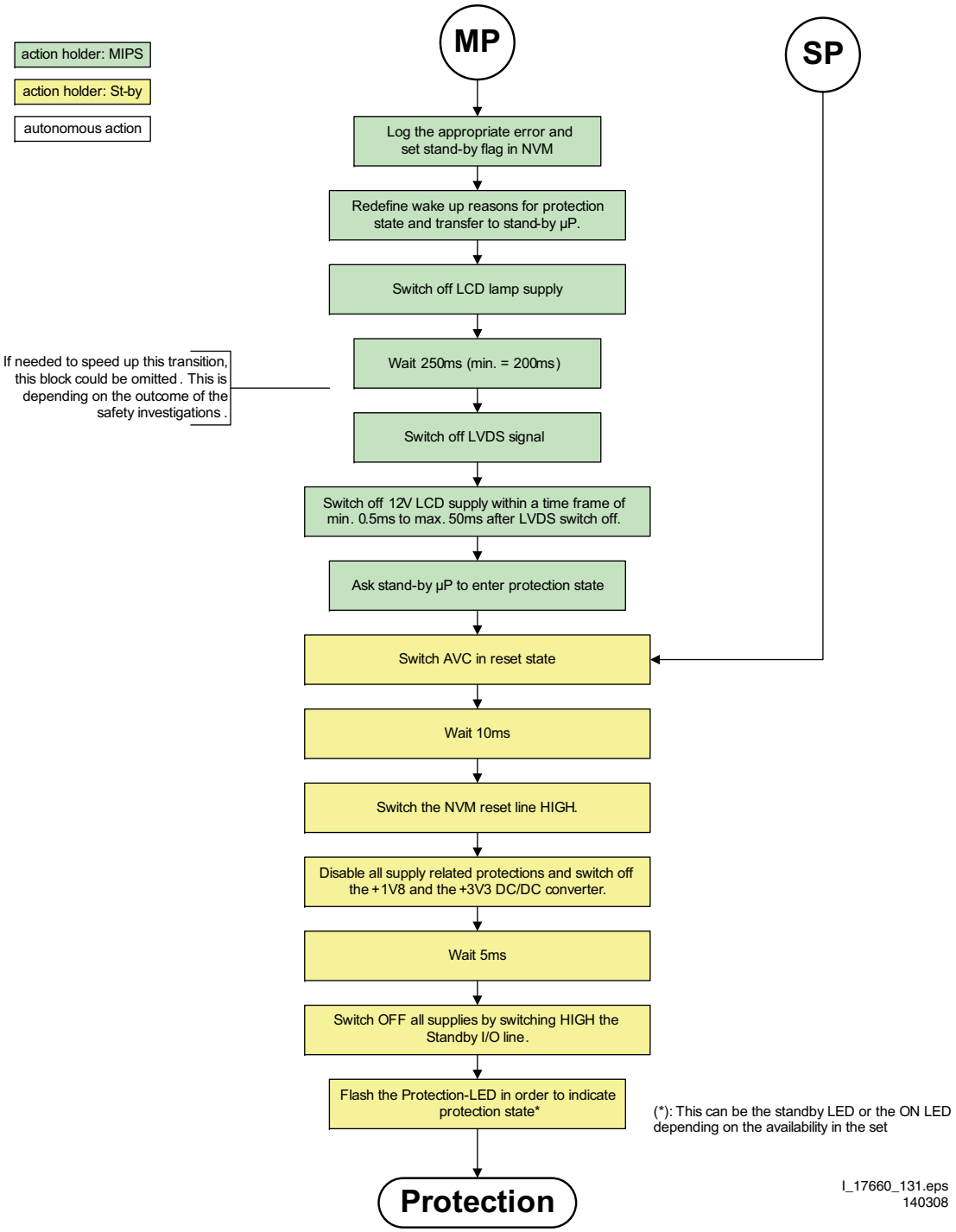


Figure 5-11 "To Protection State" flowchart

5.4 Service Tools

5.4.1 ComPair

Introduction

ComPair (Computer Aided Repair) is a Service tool for Philips Consumer Electronics products. and offers the following:

1. ComPair helps to quickly get an understanding on how to repair the chassis in a short and effective way.
2. ComPair allows very detailed diagnostics and is therefore capable of accurately indicating problem areas. No knowledge on I²C or UART commands is necessary, because ComPair takes care of this.
3. ComPair speeds up the repair time since it can automatically communicate with the chassis (when the uP is working) and all repair information is directly available.
4. ComPair features TV software up possibilities.

Specifications

ComPair consists of a Windows based fault finding program and an interface box between PC and the (defective) product. The ComPair II interface box is connected **to the PC** via an USB cable. For the TV chassis, the ComPair interface box and the TV communicate via a bi-directional cable via the service connector(s).
The ComPair fault finding program is able to determine the problem of the defective television, by a combination of automatic diagnostics and an interactive question/answer procedure.

How to Connect

This is described in the chassis fault finding database in ComPair.

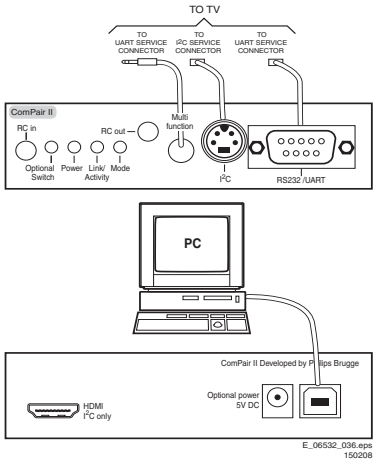


Figure 5-12 ComPair II interface connection

Caution: It is compulsory to connect the TV to the PC as shown in the picture above (with the ComPair interface in between), as the ComPair interface acts as a level shifter. If one connects the TV directly to the PC (via UART), ICs will be blown!

How to Order

ComPair II order codes:

- ComPair II interface: 3122 785 91020.
- Software is available via the Philips Service web portal.
- ComPair UART interface cable for Q54x.x. (using 3.5 mm Mini Jack connector): 3138 188 75051.

Note: While encounting problems, contact the local support desk.

5.4.2 Memory and Audio Test

With this tool you can test the memory of the PNX8543, as well if the PNX5100 is enabled and audio-testing.

What is needed?

– An USB-stick
– "TESTSCRIPT Q549". Downloadable from the Philips Service website from the section "Software for Service only"
– A ComPair/service cable (3138 188 75051).

Procedure

Create a directory "JETTFILES" under the root of the USB-stick
– Place "MemTestTV543.bin" and "autojett.bin" (available in "TESTSCRIPT Q549") under the directory "JETTFILES"
– Install the computer program "BOARDTESTLOGGER" (available in "TESTSCRIPT Q549") on the PC
– Connect a "ComPair/service"-cable from the service-connector in the set, into the "multi function" jack at the front of the ComPair II box :
Required settings in ComPair :
- start up the ComPair application.
- Select the correct database (open file "Q549.2E LA", this will set the ComPair interface in the appropriate mode).
- Close ComPair
– Start up the program "BOARDTESTLOGGER" and select "COMx"
– Put the USB stick into the TV and start up the TV while pressing the "i+"-button on a Philips DVD RC6 remote control (it's also possible to use a TV remote in "DVD"-mode)
– On the PC the memory test is shown now. This is also visible on the TV screen.
– In "BOARDTESTLOGGER" an option "Send extra UART command" can be found where you can select "AUD1". This command generates hear test tones of 200, 400, 1000, 2000, 3000, 5000, 8000 and 12500Hz.

5.5 Error Codes

5.5.1 Introduction

The error code buffer contains all detected errors since the last time the buffer was erased. The buffer is written from left to right, new errors are logged at the left side, and all other errors shift one position to the right.
When an error occurs, it is added to the list of errors, provided the list is not full. When an error occurs and the error buffer is full, then the new error is not added, and the error buffer stays intact (history is maintained).
To prevent that an occasional error stays in the list forever, the error is removed from the list after more than 50 hrs. of operation.
When multiple errors occur (errors occurred within a short time span), there is a high probability that there is some relation between them.

New in this chassis is the way errors can be displayed:

- There is a simple blinking LED procedure for board level repair (home repair) so called LAYER 1 errors next to the existing errors which are LAYER 2 errors (see Table 5-2).
  – LAYER 1 errors are one digit errors.
  – LAYER 2 errors are 2 digit errors.
- In protection mode.
  – From consumer mode: **LAYER 1.**
  – From SDM mode: **LAYER 2**.
- **Fatal errors, if I2C bus is blocked and the set reboots, CSM and SAM are not selectable.**
  – From consumer mode: **LAYER 1.**
  – From SDM mode: **LAYER 2**.
  Important remark:

For all errors detected by MIPS which are fatal => rebooting of the TV set (reboot starts after LAYER 1 error blinking), one should short the solder paths (SDM) at start-up from the power OFF state by mains interruption and not via the power button to trigger the SDM via the hardware pins.

- In CSM mode
  - When entering CSM: error **LAYER 1** will be displayed by blinking LED. Only the latest error is shown.
- In SDM mode
  - When SDM is entered via Remote Control code or the hardware pins, **LAYER 2** is displayed via blinking LED.
- In the ON state
  - In "Display error mode", set with the RC commands "mute_06250X _OK" **LAYER 2** errors are displayed via blinking LED.
- Error display on screen.
  - In CSM no error codes are displayed on screen.
  - In SAM the complete error list is shown.

Basically there are three kinds of errors:

- **Errors detected by the Stand-by software which lead to protection.** These errors will always lead to protection and an automatic start of the blinking LED LAYER 1 error. (see section "5.6 The Blinking LED Procedure").
- **Errors detected by the Stand-by software which not lead to protection.** In this case the front LED should blink the involved error. See also section "5.5 Error Codes, 5.5.4 Error Buffer, Extra Info". Note that it can take up several minutes before the TV starts blinking the error (e.g. LAYER 1 error = 2, LAYER 2 error = 15 or 53).
- **Errors detected by main software (MIPS).** In this case the error will be logged into the error buffer and can be read out via ComPair, via blinking LED method LAYER 1-2 error, or in case picture is visible, via SAM.

5.5.2 How to Read the Error Buffer

Use one of the following methods:

- On screen via the SAM (only when a picture is visible). E.g.:
  - **00 00 00 00 00**: No errors detected
  - **23 00 00 00 00**: Error code 23 is the last and only detected error.
  - **37 23 00 00 00**: Error code 23 was first detected and error code 37 is the last detected error.
  - Note that no protection errors can be logged in the error buffer.
- Via the blinking LED procedure. See section 5.5.3 How to Clear the Error Buffer.
- Via ComPair.

5.5.3 How to Clear the Error Buffer

Use one of the following methods:

- By activation of the "RESET ERROR BUFFER" command in the SAM menu.
- With a normal RC, key in sequence "MUTE" followed by "062599" and "OK".
- If the content of the error buffer has not changed for 50+ hours, it resets automatically.

5.5.4 Error Buffer

In case of non-intermittent faults, clear the error buffer before starting to repair (**before** clearing the buffer, write down the content, as this history can give significant information). This to ensure that old error codes are no longer present.
If possible, check the entire contents of the error buffer. In some situations, an error code is only the result of another error code and not the actual cause (e.g. a fault in the protection detection circuitry can also lead to a protection).
There are several mechanisms of error detection:

- Via error bits in the status registers of ICs.
- Via polling on I/O pins going to the stand-by processor.
- Via sensing of analog values on the stand-by processor or the PNX8543.
- Via a "not acknowledge" of an I^2C communication.

Take notice that some errors need several minutes before they start blinking or before they will be logged. So in case of problems wait 2 minutes from start-up onwards, and then check if the front LED is blinking or if an error is logged.

Table 5-2 Error code overview

Description	Layer 1	Layer 2	Monitored by	Error/ Prot	Error Buffer/ Blinking LED	Device	Defective Board
I^2C3	2	13	MIPS	E	BL / EB	SSB	SSB
I^2C2	2	14	MIPS	E	BL / EB	SSB/Display	SSB/display
PNX doesn't boot (HW cause) PNX 5100 doesn't boot	2	15	Stby µP	P	BL	PNX8543/PNX51XX I^2C blocked	SSB
12V	3	16	Stby µP	P	BL	/	Supply
Inverter or display supply	3	17	MIPS	E	EB	/	
1V2, 3V3, 5V to low	2	18	Stby µP	P	BL	/	SSB
Temp protection	3	12	MIPS	E	EB	/	Display
PNX 5100	2	21	MIPS	E	EB	PNX5100	SSB
HDMI mux	2	23	MIPS	E	EB	TDA9996	SSB
I^2C switch	2	24	MIPS	E	EB	PCA9540	SSB
Boot-NVM PNX5100	2	25	MIPS	E	EB	STM24C08	SSB
Multi Standard demodulator (Micronas IF)	2	27	MIPS	E	EB	DRX3616K DRX3626K	SSB
ARM (ambilight)	8	28	MIPS	E	EB	NXP LPC2103	AL module or DC/DC
FPGA (Local contrast)	2	29	MIPS	E	EB	Altera	SSB
Tuner	2	34	MIPS	E	EB	UV1783S/HD1816	SSB
Fan I2C expander	7	41	MIPS	E	EB	PCA9533	FAN module
T° sensor	7	42	MIPS	E	EB	LM 75	T° sensor
FAN 1	7	43	MIPS	E	EB		FAN
FAN 2	7	44	MIPS	E	EB		FAN
Main NVM	2	/	MIPS	E	X	STM24C128	SSB
PNX doesn't boot (SW cause)	2	53	Stby µP	E	BL	PNX8543	SSB
Display (only 56PFL9954H)	5	64	MIPS	E	BL / EB	Altera	Display

Extra Info

- **Rebooting.** When a TV is constantly rebooting due to internal problems, most of the time no errors will be logged or blinked. This rebooting can be recognized via a ComPair interface and Hyperterminal (for Hyperterminal settings, see section "5.8 Fault Finding and Repair Tips, 5.8.6 Logging). It's shown that the loggings which are generated by the main software keep continuing. In this case diagnose has to be done via ComPair.
- **Error 13 (I^2C bus 3 blocked)**. At the time of release of this manual, this error was not working as expected. Current situation: when this error occurs, the TV will constantly reboot due to the blocked bus. The best way for further diagnosis here, is to use ComPair.
- **Error 15 (PNX8543,PNX5100 doesn't boot)**. Indicates that the main processor/PNX5100 was not able to read his bootscript. This error will point to a hardware problem around the PNX8543 (supplies not OK, PNX 8543 completely dead, I^2C link between PNX and Stand-by Processor broken, etc...). When error 15 occurs it is also possible that I^2C1 bus is blocked (NVM). I^2C1 can be indicated in the schematics as follows: SCL-UP-MIPS, SDA-UP-MIPS, SCL-1, SDA-1, SCL-2 or SDA-2. Other root causes for this error can be due to hardware problems from the NVM PNX5100, DDR's and the bootscript reading from the PNX5100.
- **Error 16 (12V)**. This voltage is made in the power supply and results in protection (LAYER 1 error = 3) in case of absence. When SDM is activated we see blinking LED LAYER 2 error = 16.
- **Error 17 (Invertor or Display Supply)**. Here the status of the "Power OK" is checked by software, no protection will occur during failure of the invertor or display supply (no picture), only error logging. LED blinking of LAYER 1 error = 3 in CSM, in SDM this gives LAYER 2 error = 17.
- **Error 18 (1V2-3V3-5V too low)**. All these supplies are generated by the DC/DC supply on the SSB. If one of these supplies is too low, protection occurs and blinking LED LAYER 1 error = 2 will be displayed automatically. In SDM this gives LAYER 2 error = 18.
- **Error 21 (PNX 5100)**. When there is no I^2C communication towards the PNX5100, the TV set will start rebooting and display LAYER 1 error = 2. Disconnect the mains cord now and start up the TV set with the solder path (SDM) short to ground during start-up to activate the LAYER 2 error blinking. Error "21" will be logged and displayed via the blinking LED procedure after a few moments from start-up. Remark : the rebooting can be recognized via a ComPair interface and Hyperterminal (for Hyperterminal settings, see section "5.8 Fault Finding and Repair Tips, 5.8.6 Logging"). It is shown that the loggings which are generated by the main software keep continuing. Check in the logging for keywords like e.g. "Device error 21".
- **Error 23 (HDMI)**. When there is no I^2C communication towards the HDMI mux after start-up, LAYER 2 error = 23 will be logged and displayed via the blinking LED procedure if SDM is switched on. It should be noted that in case a new spare EDID MUX device is used for repair, the initial default address must be changed from "C0" to "CE", to be done via ComPair.
- **Error 24 (I^2C switch)**. When there is no I^2C communication towards the I^2C switch, LAYER 2 error = 24 will be logged and displayed via the blinking LED procedure when SDM is switched on. Remark : this only works for TV sets with an I^2C controlled screen included.
- **Error 25 (Boot-NVM PNX5100)**. Same behaviour as described in "Error 21 (PNX5100)".
- **Error 27 (Micronas IF)**. When there is no I^2C communication towards the multi standard demodulator, LAYER 2 error = 27 will be logged and displayed via the blinking LED procedure if SDM is switched on.
- **Error 28 (ARM ambilight)**. When there is no I^2C communication towards the ARM processor, LAYER 2 error = 28 will be logged and displayed via the blinking LED procedure if SDM is switched on.
- **Error 29 (FPGA local contrast)**. When there is no I^2C communication towards this FPGA, LAYER 2 error = 29 will be logged and displayed via the blinking LED procedure if SDM is activated.
- **Error 34 (Tuner)**. When there is no I^2C communication towards the tuner after start-up, LAYER 2 error = 34 will be

logged and displayed via the blinking LED procedure when SDM is switched on.
- **Error 42 (Temp sensor)**. Only applicable for TV sets with an I²C controlled screen.
- **Main NVM**. When there is no I²C communication towards the main NVM, LAYER 1 error = 2 will be displayed via the blinking LED procedure. In SDM, LAYER 2 error will be blinked as "15". Errors here can not be logged due to inaccessibility of the NVM device.
- **Error 53**. This error will indicate that the PNX8543 has read his bootscript (when this would have failed, error 15 would blink) but initialization was never completed because of hardware problems (NAND flash, ...) or software initialization problems. Possible cause could be that there is no valid software loaded (try to upgrade to the latest main software version). Note that it can take a few minutes before the TV starts blinking LAYER 1 error = 2 or in SDM, LAYER 2 error = 53.
- **Error 64**. Only applicable for TV sets with an I²C controlled screen .

5.6 The Blinking LED Procedure

5.6.1 Introduction

The blinking LED procedure can be split up into two situations:
- Blinking LED procedure LAYER 1 error. In this case the error is automatically blinked when the TV is put in CSM. This will be only one digit error, namely the one that is referring to the defective board (see table "5-2 Error code overview") which causes the failure of the TV. This approach will especially be used for home repair and call centres. The aim here is to have service diagnosis from a distance.
- Blinking LED procedure LAYER 2 error. Via this procedure, the contents of the error buffer can be made visible via the front LED. In this case the error contains 2 digits (see table "5-2 Error code overview") and will be displayed when SDM (hardware pins) is activated. This is especially useful for fault finding and gives more details regarding the failure of the defective board.

Important remark:
For all errors detected by MIPS which are fatal => rebooting of the TV set (reboot starts after LAYER 1 error blinking), one should short the solder paths at start-up from the power OFF state by mains interruption and not via the power button to trigger the SDM via the hardware pins.

When one of the blinking LED procedures is activated, the front LED will show (blink) the contents of the error buffer. Error codes greater then 10 are shown as follows:
1. "n" long blinks (where "n" = 1 to 9) indicating decimal digit
2. A pause of 1.5 s
3. "n" short blinks (where "n"= 1 to 9)
4. A pause of approximately 3 s,
5. When all the error codes are displayed, the sequence finishes with a LED blink of 3 s
6. The sequence starts again.

Example: Error 12 8 6 0 0.
After activation of the SDM, the front LED will show:
1. One long blink of 750 ms (which is an indication of the decimal digit) followed by a pause of 1.5 s
2. Two short blinks of 250 ms followed by a pause of 3 s
3. Eight short blinks followed by a pause of 3 s
4. Six short blinks followed by a pause of 3 s
5. One long blink of 3 s to finish the sequence
6. The sequence starts again.

5.6.2 How to Activate

Use one of the following methods:
- **Activate the CSM**. The blinking front LED will show only the latest layer 1 error, this works in "normal operation" mode or automatically when the error/protection is monitored by the standby processor.
  In case no picture is shown and there is no LED blinking, read the logging to detect whether "error devices" are mentioned. (see section "5.8 Fault Finding and Repair Tips, 5.8.6 Logging").
- **Activate the SDM**. The blinking front LED will show the entire content of the LAYER 2 error buffer, this works in "normal operation" mode or when SDM (via hardware pins) is activated when the tv set is in protection.
  Important remark:
  For all errors detected by MIPS which are fatal => rebooting of the TV set (reboot starts after LAYER 1 error blinking), one should short the solder paths at start-up from the power OFF state by mains interruption and not via the power button to trigger the SDM via the hardware pins.
- **Transmit the commands "MUTE" - "062500" - "OK" with a normal RC**. The complete error buffer is shown. Take notice that it takes some seconds before the blinking LED starts.
- **Transmit the commands "MUTE" - "06250x" - "OK" with a normal RC** (where "x" is a number between 1 and 5). When x = 1 the last detected error is shown, x = 2 the second last error, etc.... Take notice that it takes some seconds before the blinking LED starts.

5.7 Protections

5.7.1 Software Protections

Most of the protections and errors use either the stand-by microprocessor or the MIPS controller as detection device. Since in these cases, checking of observers, polling of ADCs, and filtering of input values are all heavily software based, these protections are referred to as software protections. There are several types of software related protections, solving a variety of fault conditions:
- **Protections related to supplies:** check of the 12V, +5V, +3V3 and 1V2.
- **Protections related to breakdown of the safety check mechanism.** E.g. since the protection detections are done by means of software, failing of the software will have to initiate a protection mode since safety cannot be guaranteed any more.

Remark on the Supply Errors
The detection of a supply dip or supply loss during the normal playing of the set does not lead to a protection, but to a cold reboot of the set. If the supply is still missing after the reboot, the TV will go to protection.

Protections during Start-up
During TV start-up, some voltages and IC observers are actively monitored to be able to optimise the start-up speed, and to assure good operation of all components. If these monitors do not respond in a defined way, this indicates a malfunction of the system and leads to a protection. As the observers are only used during start-up, they are described in the start-up flow in detail (see section "5.3 Stepwise Start-up").

5.7.2 Hardware Protections

The only real hardware protection in this chassis appears in case of an audio problem e.g. DC voltage on the speakers. This protection will only affect the Class D (7D10) and puts the amplifier in a continuous burst mode (cyclus approximately 2 seconds).

Repair Tip
- There will be still picture available but no sound. While the Class D amplifier tries to start-up again, the cone of the

loudspeakers will move slowly in one or the other direction until the initial failure shuts the amplifier down, this cyclus starts over and over again.

5.7.3 Important remark regarding the blinking LED indication

As for the blinking LED indication, the blinking led of LAYER 1 error displaying can be switched off by pushing the power button on the keyboard.
This condition is not valid after the set was unpowered (via mains interruption). The blinking LED starts again and can only be switched off by unplugging the mains connection.
This can be explained by the fact that the MIPS can not load the keyboard functionality from software during the start-up and doesn't recognizes the keyboard commands at this time.

5.8 Fault Finding and Repair Tips

Read also section "5.5 Error Codes, 5.5.4 Error Buffer, Extra Info".

5.8.1 Ambilight

Due to degeneration process of the AmbiLights, there can be a difference in the colour and/or light output of the spare ambilight module in comparison with the originals ones contained in the TV set. Via ComPair the light output can be adjusted.

5.8.2 Audio Amplifier

The Class D-IC 7D10 has a powerpad for cooling. When the IC is replaced it must be ensured that the powerpad is very well pushed to the PWB while the solder is still liquid. This is needed to insure that the cooling is guaranteed, otherwise the Class D-IC could break down in short time.

5.8.3 CSM

When CSM is activated and there is a USB stick connected to the TV, the software will dump the complete CSM content to the USB stick. The file (Csm.txt) will be saved in the root of the USB stick. If this mechanism works it can be concluded that a large part of the operating system is already working (MIPS, USB...)

5.8.4 DC/DC Converter

Description

The onboard supply consists of 5 DC/DC converters and 4 linear stabilizers. All DC/DC converters have +12V input voltage and deliver :

- +1V2-PNX85XX supply voltage (1.24V nominal), stabilized close to PNX8543 chip.
- +1V2-PNX5120 supply voltage (1.26V nominal), stabilized close to PNX5120 chip.
- +3V3 (3.34V nominal, overall 3.3 V for onboard IC's).
- +5V (5.15V nominal) for USB and Conditional Access Interface and +5V5-TUN for +5V-TUN tuner stabilizer.
- +33VTUN (34V nominal) for analog-only tuners.

The linear stabilizers are providing:

- +1V2-STANDBY (out of +3V3-STANDBY), 1.24V nominal.
- +1V8-PNX85XX and +1V8PNX5100 (connected via CFH1), 1.84V nominal.
- +2V5 (WOW FPGA diversity only), 2.5V nominal.
- +5V-TUN (out of +5V5-TUN), 5V nominal.

+3V3-STANDY and +1V2-STANDBY are permanent voltages. Supply voltages +1V2-PNX85XX and +1V2-PNX5100 are started immediately when +12V incoming voltage is available (+12V is enabled by STANDBY signal, active low). Supply voltages +3V3, 2V5, +1V8-PNX5100, +1V8-PNX85XX, +5V and +5V-TUN are switched-on directly by signal ENABLE-3V3 (active low), provided that +12V (detected via 7U40 &7U41) is available. +12V is considered OK (=> DETECT -12V signal becomes high and 12V/3V3 and 12V/5V DC-DC converter can be started up) if it rises above 10V5 (typical) and doesn't drop below 10V (typical).

Debugging

The best way to find a failure in the DC/DC converters is to check their start-up sequence at power-on via the mains cord, presuming that the standby microprocessor and the external supply are operational. Take STANDBY signal high-to-low transition as time reference.
When +12V becomes available (maximum 1 second after STANDBY signal goes low) then +1V2-PNX85XX and +1V2-PNX5100 are started immediately. Then, after ENABLE-3V3 goes low, all the other supply voltages should rise within 2ms.

Tips

- When an output supply voltage is short-circuited to GND the corresponding DC-DC converter is not making any audible noise, the converter switches-off immediately and will attempt a re-start only after +12V drops and rises again.
- Check the integrity (at least no short-circuit between drain and source) of power MOS-FETs, especially the high-side ones: 7U05, 7U08, 7U0D-1 and 7U0H-1 before starting the platform in SDM mode, otherwise it can be easily damaged.
- Switching frequency of DC-DC converters should be around 290KHz for 12V to 1V2 DC-DC converters and around 370KHz for 12V to 3V3 and 12V to 5V DC-DC converters.

5.8.5 Exit "Factory Mode"

When an "F" is displayed in the screen's right corner, this means the set is in "Factory" mode, and it normally happens after a new SSB is mounted. To exit this mode, push the "VOLUME minus" button on the TV's local keyboard for 10 seconds (this disables the continuous mode).
Then push the "SOURCE" button for 10 seconds until the "F" disappears from the screen.

5.8.6 Logging

When something is wrong with the TV set (f.i.the set is rebooting) you can check for more information via the logging in Hyperterminal. The Hyperterminal is available in every Windows application via Programs, Accessories, Communications, Hyperterminal. Connect a "ComPair UART"-cable (3138 188 75051) from the service connector in the TV to the "multi function" jack at the front of ComPair II box.
Required settings in ComPair before starting to log :
- Start up the ComPair application.
- Select the correct database (open file "Q549.2E LA", this will set the ComPair interface in the appropriate mode).
- Close ComPair

After start-up of the Hyperterminal, fill in a name (f.i. "logging") in the "Connection Description" box, then apply the following settings:
1. COMx
2. Bits per second = 115200
3. Data bits = 8
4. Parity = none
5. Stop bits = 1
6. Flow control = none

During the start-up of the TV set, the logging will be displayed. This is also the case during rebooting of the TV set (the same logging appears time after time). Also available in the logging is the "Display Option Code" (useful when there is no picture),

look for item “DisplayRawNumber” in the beginning of the logging. Tip: when there is no picture available during rebooting you are able to check for “error devices” in the logging (LAYER 2 error) which can be very helpful to determine the failure cause of the reboot. For protection state, there is no logging.

5.8.7 Loudspeakers

Make sure that the volume is set to minimum during disconnecting the speakers in the ON-state of the TV. The audio amplifier can be damaged by disconnecting the speakers during ON-state of the set!

5.8.8 IPB

In case of no picture when CSM-test pattern from PNX5100 is activated and backlight doesn’t light up, it’s recommended first to check the inverter on the IPB + wiring (LAYER 2 error = 17 is displayed in SDM).

5.8.9 Tuner

Attention: In case the tuner is replaced, always check the tuner options!

5.8.10 PCI bus

The splash screen image is not distributed via the regular YUV signal path from the PNX8543 to the PNX51XX, but loaded one time via the PCI bus.Once the splash screen image is loaded into the PNX51XX, it will be continuously generated by the PNX51XX until the first incoming video disables the splash screen.So when teletext and/or general UI is available, but no splash screen (option “ON”) is visible during start-up, check the PCI bus as possible root cause.

5.8.11 Display option code

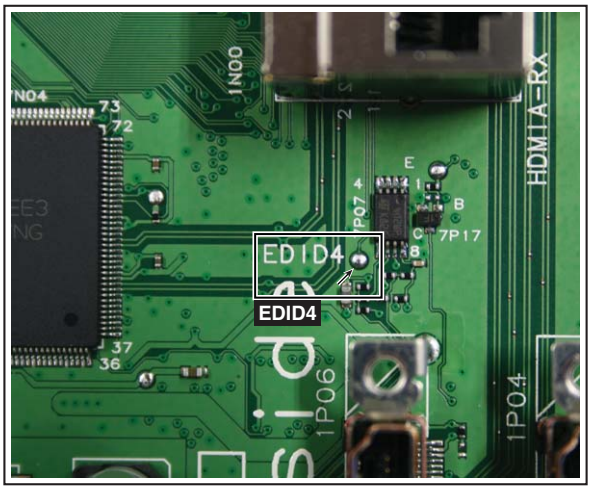
Attention: In case the SSB is replaced, always check the display option code in SAM, even when picture is available. Performance with the incorrect display option code can lead to unwanted side-effects for certain conditions.

5.8.12 Upgrade HDMI EDID NVM

The EDID MUX device (including all HDMI NVM except the 4th) is upgradeable via USB, see ComPair for further instructions. It should be noted that in case a new spare EDID MUX device is used for repair, the initial default address must be changed from “C0” to “CE”, to be done via ComPair.

5.8.13 Upgrade VGA/4th HDMI EDID NVM

The EDID for VGA connector or the 4th HDMI can only be upgraded via external I^2C. To upgrade the EDID for the VGA connector or 4th HDMI, pin 7 of the EDID NVM has to be short circuited to ground. Therefore a test point is foreseen (see Figure 5-13). For the VGA EDID NVM it’s most suitable to connect pin 7 to ground on the NVM device itself. See ComPair for further instructions.



18310_220_090318.eps
090319

Figure 5-13 4th HDMI EDID NVM pin

5.8.14 Wi-Fi module

To prevent damage on the coax wires, especially the female core of the coax wires (can be bend over during dis- and reconnecting), this should be carried out by use of pliers.

5.8.15 SSB Replacement

Follow the instructions in the flowchart in case a SSB has to be exchanged. See figure “SSB replacement flowchart”.

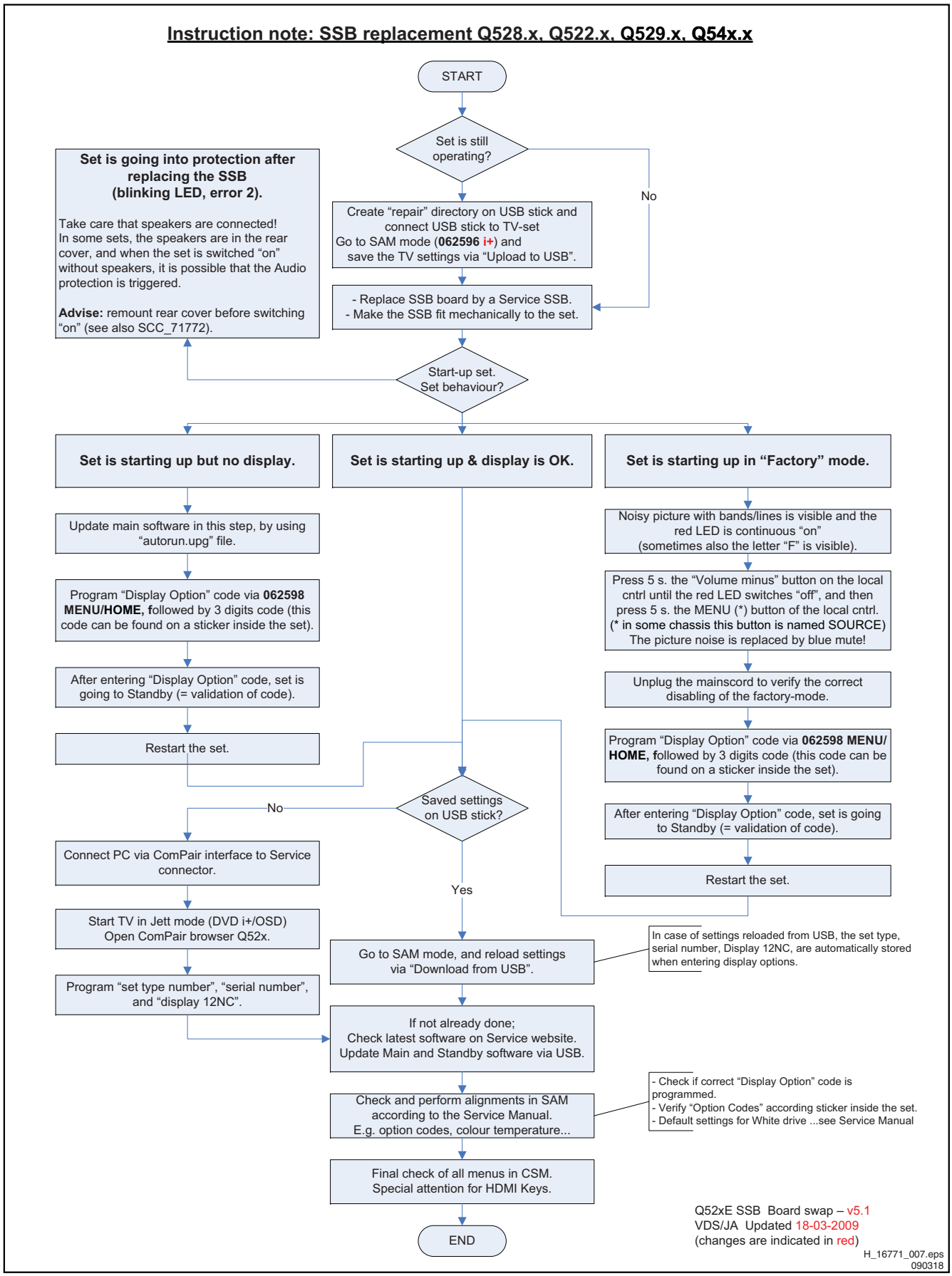


Figure 5-14 SSB replacement flowchart

5.9 Software Upgrading

5.9.1 Introduction

The set software and security keys are stored in a NAND-Flash, which is connected to the PNX8543 via the PCI bus.

It is possible **for the user** to upgrade the **main** software via the USB port. This allows replacement of a software image in a stand alone set, without the need of an E-JTAG debugger. A description on how to upgrade the main software can be found in the DFU.

Important: When the NAND-Flash must be replaced, a new SSB must be ordered, due to the presence of the security keys! (copy protection keys, MAC address, ...).
Perform the following actions after SSB replacement:
1. Set the correct option codes (see sticker inside the TV).
2. Update the TV software => see the eUM (electronic User Manual) for instructions.
3. Perform the alignments as described in chapter 6 (section 6.5 Reset of Repaired SSB).
4. Check in CSM if the HDMI key, MAC address.. are valid.

For the correct order number of a new SSB, always refer to the Spare Parts list!

5.9.2 Main Software Upgrade

- The “UpgradeAll.upg” file is only used in the factory.
- The “FlashUtils.upg” file is only used by service centra which are allowed to do component level repair on the SSB.

Automatic Software Upgrade
In “normal” conditions, so when there is no major problem with the TV, the main software and the default software upgrade application can be upgraded with the “AUTORUN.UPG” (FUS part of the one-zip file: e.g. 3104 337 05661 _FUS _Q5492_ 1.26.15.0_commercial.zip). This can also be done by the consumers themselves, but they will have to get their software from the commercial Philips website or via the Software Update Assistant in the user menu (see eUM). The “autorun.upg” file must be placed in the root of the USB stick.
How to upgrade:
1. Copy “AUTORUN.UPG” to the root of the USB stick.
2. Insert USB stick in the set while the set is in ON MODE. The set will restart and the upgrading will start automatically. As soon as the programming is finished, a message is shown to remove the USB stick and restart the set.

Manual Software Upgrade
In case that the software upgrade application does not start automatically, it can also be started manually.
How to start the software upgrade application manually:
1. Disconnect the TV from the Mains/AC Power.
2. Press the “OK” button on a Philips TV remote control or a Philips DVD RC-6 remote control (it is also possible to use a TV remote in “DVD” mode). Keep the “OK” button pressed while reconnecting the TV to the Mains/AC Power.
3. The software upgrade application will start.

Attention!
In case the download application has been started **manually**, the “autorun.upg” will maybe not be recognized.
What to do in this case:
1. Create a directory “UPGRADES” on the USB stick.
2. Rename the “autorun.upg” to something else, e.g. to “software.upg”. Do not use long or complicated names, keep it simple. Make sure that “AUTORUN.UPG” is no longer present in the root of the USB stick.
3. Copy the renamed “upg” file into this directory.
4. Insert USB stick into the TV.
5. The renamed “upg” file will be visible and selectable in the upgrade application.

Back-up Software Upgrade Application
If the default software upgrade application does not start (could be due to a corrupted boot 2 sector) via the above described method, try activating the “back-up software upgrade application”.
How to start the “back-up software upgrade application” manually:
1. Disconnect the TV from the Mains/AC Power.
2. Press the “INFO”-button on a Philips remote control or “CURSOR DOWN” button on a Philips DVD RC-6 remote control (it is also possible to use a TV remote in “DVD” mode). Keep the “INFO”-button (or “cursor down” button) pressed while reconnecting the TV to the Mains/AC Power.
3. The software upgrade application will start.

5.9.3 Stand-by Software Upgrade via USB

In this chassis it is possible to upgrade the Stand-by software via a USB stick. The method is similar to upgrading the main software via USB.
Use the following steps:
1. Create a directory “UPGRADES” on the USB stick.
2. Copy the Stand-by software (part of the one-zip file, e.g. StandbySW_CFT72_88.0.0.0.upg) into this directory.
3. Insert the USB stick into the TV.
4. Start the download application manually (see section “ Manual Software Upgrade”.
5. Select the appropriate file and press the “OK” button to upgrade.

5.9.4 Content and Usage of the One-Zip Software File

Below the content of the One-Zip file is explained, and instructions on how and when to use it.

- **BootProm_PNX5120_Q5492_x.x.x.x.zip.** A programmed device can be ordered via the regional Service organization.
- **Ceisp2padII_P2PAD_x.x.x.x.zip.** Not to be used by Service technicians. For ComPair development only.
- **DDC_Q5492_x.x.x.x.zip.** Contains the content of the VGA NVM. See ComPair for further instruction.
- **EDID_Q5492_x.x.x.x.zip.** Contains the EDID content of the different EDID NVM’s. See ComPair for further instructions.
- **EJTAGDownload_Q5492_x.x.x.x.zip.** Only used by service centra which are allowed to do component level repair.
- **FUS_Q5492_x.x.x.x_commercial.zip.** Contains the “autorun.upg” which is needed to upgrade the TV main software and the software download application.
- **Factory_Q5492_x.x.x.x_commercial.zip.** Only for production purposes, not to be used by Service technicians.
- **FlashUtils_Q5492_x.x.x.x_commercial.zip.** Not to be used by Service technicians.
- **MOP_RAC3_x.x.x.x.zip.** Contains the MOP local contrast software and is upgradeable via USB (UPG). This SW is not part of the FUS autorun.upg!
- **OAD_Q5492_x.x.x.x.zip.** Not to be used by Service Technicians.
- **OpenSourceFile_Q5492_x.x.x.x.zip.** Not to be used by Service technicians.
- **PQPrivate_Q5492_x.x.x.x.zip.** Not to be used by Service technicians.
- **StandbySW_CFTxx_x.x.x.x_commercial.zip.** Contains the Stand-by software in “upg” and “hex” format.
  - The “StandbySW_xxxxx_prod.upg” file can be used to upgrade the Stand-by software via USB.
  - The “StandbySW_xxxxx.hex” file can be used to upgrade the Stand-by software via ComPair.

  - The files “StandbySW_xxxxx_exhex.hex” and “StandbySW_xxxxx_dev.upg” may not be used by Service technicians (only for development purposes).
- **UpgradeAll_Q5492_x.x.x.x_commercial.zip.** Only for production purposes, not to be used by Service technicians.
  Caution: Never try to use this file, because it will overwrite the HDCP keys ! ! !
- **UpgradeExe_Q5492X_x.x.x.x.zip.** Not to be used by Service Technicians.
- **Ambilight_Q5492_x.x.x.x.zip.** Not to be used by Service technicians.
- **Cabinet_Q5492_x.x.x.x.zip**. Not to be used by Service technicians.
- **Display_Q5492_x.x.x.x.zip**. Not to be used by Service technicians.
- **LightGuide_TV522_x.x.x.x_.zip.** Not to be used by Service Technicians.
- **ProcessNVM_Q5492_x.x.x.x.zip.** Default NVM content. Must be programmed via ComPair or can be loaded via USB, be aware that all alignments stored in NVM are overwritten here.

5.9.5 Content of the MOP Ambilight ARM SW File

- MOP_AMBILIGHT_V1-2_UPG_jettsigned.zip. Contains the MOP ambientlight software (ARM processor on the DC-DC AL interface board) and is upgradeable via USB (UPG). This SW is not part of the FUS autorun.upg! and is not available in the One-Zip software file but provided separately via the commercial Philips website (software for servicers only). Instructions for upgrading are included in the zip file.

5.9.6 UART logging 2K9 (see section “5.8 Fault Finding and Repair Tips, 5.8.6 Logging)

6. Alignments

Index of this chapter:

6.1 General Alignment Conditions

Perform all electrical adjustments under the following conditions:

- Power supply voltage (depends on region):
  - **AP-NTSC:** 120 VAC or 230 V_{AC} / 50 Hz (± 10%).
  - **AP-PAL-multi:** 120 - 230 V_{AC} / 50 Hz (± 10%).
  - **EU:** 230 V_{AC} / 50 Hz (± 10%).
  - **LATAM-NTSC:** 120 - 230 V_{AC} / 50 Hz (± 10%).
  - **US:** 120 V_{AC} / 60 Hz (± 10%).
- Connect the set to the mains via an isolation transformer with low internal resistance.
- Allow the set to warm up for approximately 15 minutes.
- Measure voltages and waveforms in relation to correct ground (e.g. measure audio signals in relation to AUDIO_GND).
  Caution: It is not allowed to use heat sinks as ground.
- Test probe: Ri > 10 MΩ, Ci < 20 pF.
- Use an isolated trimmer/screwdriver to perform alignments.

6.1.1 Alignment Sequence

- First, set the correct options:
  - In SAM, select “Options”, and then “Option numbers”.
  - Fill in the option settings for “Group 1” and “Group 2” according to the set sticker (see also paragraph 6.4 Option Settings).
  - Press OK on the remote control before the cursor is moved to the left.
  - In submenu “Option numbers” select “Store” and press OK on the RC.
- OR:
  - In main menu, select “Store” again and press OK on the RC.
  - Switch the set to Stand-by.
- Warming up (>15 minutes).

6.2 Hardware Alignments

Not applicable.

6.3 Software Alignments

Put the set in SAM mode (see Chapter 5. Service Modes, Error Codes, and Fault Finding). The SAM menu will now appear on the screen. Select ALIGNMENTS and go to one of the sub menus. The alignments are explained below.
The following items can be aligned:

- Tuner AGC.
- White point.

To store the data:

- Press OK on the RC **before the cursor is moved to the left**.
- In main menu select “Store” and press OK on the RC.
- Press MENU on the RC to switch back to the main menu.
- Switch the set to stand-by mode.

For the next alignments, supply the following test signals via a video generator to the RF input:

- **EU/AP-PAL models:** a PAL B/G TV-signal with a signal strength of at least 1 mV and a frequency of 475.25 MHz
- **US/AP-NTSC models:** an NTSC M/N TV-signal with a signal strength of at least 1 mV and a frequency of 61.25 MHz (channel 3).
- **LATAM models:** an NTSC M TV-signal with a signal strength of at least 1 mV and a frequency of 61.25 MHz (channel 3).

6.3.1 Tuner AGC (RF AGC Take Over Point Adjustment)

Purpose: To keep the tuner output signal constant as the input signal amplitude varies.
No alignment is necessary, for the AGC alignment you can use the default value : “80”.
Store settings and exit SAM.

6.3.2 White Point

- Set “Active control” to “Off”.
- Choose “TV menu”, “TV Settings” and then “Picture” and set picture settings as follows:

Picture Setting	
Dynamic backlight	Off
Dynamic Contrast	Off
Colour Enhancement	Off
Picture Format	Unscaled
Light Sensor	Off
Brightness	50
Colour	0
Contrast	100

- Go to the SAM and select “Alignments”-> “White point”.

White point alignment LCD screens:

- Use a 100% white screen as input signal and set the following values:
  - “Colour temperature”: “Normal”.
  - All “White point” values to: “127”.
  - “Red BL offset” values to “8”.
  - “Green BL offset” values to “8”.

In case you have a colour analyser:

- Measure with a calibrated contactless colour analyser in the centre of the screen. Consequently, the measurement needs to be done in a dark environment.
- Adjust the correct x,y coordinates (while holding one of the White point registers R, G or B on 127) by means of decreasing the value of one or two other white points to the correct x,y coordinates (see Table 6-1 White D alignment values). Tolerance: dx: ± 0.004, dy: ± 0.004.
- Repeat this step for the other colour temperatures that need to be aligned.
- When finished press OK on the RC and then press STORE (in the SAM root menu) to store the aligned values to the NVM.
- Restore the initial picture settings after the alignments.

Table 6-1 White D alignment values

Value	Cool (11000K)	Normal (9000K)	Warm (6500K)
x	0.270	0.279	0.309
y	0.279	0.287	0.328

If you do not have a colour analyser, you can use the default values. This is the next best solution. The default values are average values coming from production.

- Select a COLOUR TEMPERATURE (e.g. COOL, NORMAL, or WARM).

- Set the RED, GREEN and BLUE default values according to the values in Table 6-2.
- When finished press OK on the RC, then press STORE (in the SAM root menu) to store the aligned values to the NVM.
- Restore the initial picture settings after the alignments.

Table 6-2 White tone default setting

White Tone	32"			37"			Black level offset	
Colour Temp	R	G	B	R	G	B	R	G
Normal	127	95	97	127	121	106	8	8
Cool	127	100	112	124	127	119	8	8
Warm	127	89	52	127	111	64	8	8

White Tone	56"			Black level offset	
Colour Temp	R	G	B	R	G
Normal	127	117	111	8	8
Cool	124	124	125	8	8
Warm	127	95	65	8	8

6.4 Option Settings

6.4.1 Introduction

The microprocessor communicates with a large number of I2C ICs in the set. To ensure good communication and to make digital diagnosis possible, the microprocessor has to know which ICs to address. The presence / absence of these PNX5100 ICs (back-end advanced video picture improvement IC which offers motion estimation and compensation features (commercially called HDNM) plus integrated Ambilight control) is made known by the option codes.

Notes:
- After changing the option(s), save them by pressing the OK button on the RC before the cursor is moved to the left, select STORE in the SAM root menu and press OK on the RC.
- The new option setting is only active after the TV is switched “off” / “stand-by” and “on” again with the mains switch (the NVM is then read again).

6.4.2 Dealer Options

For dealer options, in SAM select “Dealer options”.
See Table 6-4 SAM mode overview.

6.4.3 (Service) Options

Select the sub menu's to set the initialisation codes (options) of the model number via text menus.
See Table 6-4 SAM mode overview.

6.4.4 Opt. No. (Option numbers)

Select this sub menu to set all options at once (expressed in two long strings of numbers).
An option number (or “option byte”) represents a number of different options. When you change these numbers directly, you can set all options very quickly. All options are controlled via eight option numbers.
When the NVM is replaced, all options will require resetting. To be certain that the factory settings are reproduced exactly, you must set both option number lines. You can find the correct option numbers on a sticker inside the TV set and in Table 6-3 Option and display code overview.
Example: The options sticker gives the following option numbers:
- 08192 00133 01387 45160
- 12232 04256 00164 00000

The first line (group 1) indicates hardware options 1 to 4, the second line (group 2) indicate software options 5 to 8.
Every 5-digit number represents 16 bits (so the maximum value will be 65536 if all options are set).
When all the correct options are set, the sum of the decimal values of each Option Byte (OB) will give the option number.
See Table 6-3 Option and display code overview for the options.

Diversity
Not all sets with the same Commercial Type Number (CTN) necessarily have the same option code!
Use of Alternative BOM => an alternative BOM number usually indicates the use of an alternative display or power supply. This results in another display code thus in another Option code. For the power supply there is no difference. Refer to Chapter 2. Technical Specifications and, Connections.

6.4.5 Option Code Overview

Table 6-3 Option and display code overview

CTN	Options Group 1	Options Group 2	Disp. code
32PFL9604H/12	08211 35971 18431 45288	30645 47282 00184 00000	181
32PFL9604H/60	08211 35971 18431 45288	30645 47282 00184 00000	181
37PFL9604H/12	08227 35972 18431 45288	30625 47282 00176 00000	161
37PFL9604H/60	08227 35972 18431 45288	30625 47282 00176 00000	161
56PFL9954H/12	08275 33925 18431 45288	30644 47282 00161 00000	180

Important: after having edited the option numbers as described above, you **must press OK** on the remote control **before the cursor is moved to the left**!

6.5 Reset of Repaired SSB

A very important issue towards a repaired SSB from a service repair shop implies the reset of the NVM on the SSB.
A repaired SSB in service should get the service Set type “00PF0000000000” and Production code “00000000000000”. Also the virgin bit is to be set. To set all this, you can use the ComPair tool.
In case of a display replacement, reset the “Operation hours display” to “0”, or to the operation hours of the replacement display.

New here in this chassis is the “Net TV” functionality. Therefore the CTN (“set type” item in CSM1) must be filled into the spare SSB to ensure access to the Net TV portals.
The loading of the CTN can be done via ComPair (Model number programming).
The reset item (Clear NET TV memory) can be selected via MENU (or HOME) => Setup => Installation => Clear NET TV memory (customer preferences stored at provider side will be reset now).

6.5.1 SSB identification

Whenever ordering a new SSB, it should be noted that the correct ordering number (12nc) of a SSB is located on a sticker on the SSB. The format is <12nc SSB><serial number>. The ordering number of a “Service” SSB is the same as the ordering number of an initial “factory” SSB.

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090319

Figure 6-1 SSB identification

6.6 Service SSB delivered without main software loaded

Due to a changed manufacturing process, new **Service SSB’s can be delivered** to the warehouse **without main TV software** loaded. Below you find the steps to follow when such an SSB is received.

6.6.1 When a picture is available

1. Mount the Service SSB into the TV set. After start-up, normally the download application will appear on the screen.
2. Download the latest main software (FUS) from the www.p4c.philips.com website.
3. Create a folder "upgrades" in the root of a USB stick (size > 50 MB) and save the "autorun.upg" file in this "upgrades" folder. **Note:** it is possible to rename this file, e.g. "Q549_SW_version.upg", this in case there are more than one "autorun.upg" files on your USB stick
4. Plug the prepared USB stick into the TV set, and select the "autorun" file in the displayed browser on the screen
5. Now the main TV software will be loaded automatically, supported by a progress bar
6. Set the correct "display code" via "062598-HOME-xxx", where "xxx" is the 3-digit display panel code (see sticker on the side/bottom of the cabinet).

6.6.2 When no picture is available

Due to a possible wrong display option code in the received Service SSB (NVM), no picture can be available at start-up and thus no download application will be visible. Here you can proceed and finalize step by step to load the main TV software via the UART logging on the PC (for visual feedback).

1. Start-up the TV set, equipped with the Service SSB, and enable the UART logging on the PC (see for settings 5.8 Fault Finding and Repair Tips 5.8.6 Logging)
2. The TV set will start-up automatically in the download application if main TV software is not loaded
3. Plug the prepared USB stick into the TV set, press cursor "Right" to enter the list, and navigate to the "autorun" file in the UART logging printout via the cursor keys on the remote control. When the correct file is selected, press "OK"
4. Press cursor "Down" and "OK" to start the flashing of the main TV software. Printouts like: "L: 1-100% , V: 1-100% and P: 1-100%" should be visible now in the UART logging
5. Wait until the message "Operation successful!” is displayed and remove all inserted media. Restart the TV set
6. Set the correct "display code" via "062598-HOME-xxx", where "xxx" is the 3-digit display panel code (see sticker on the side/bottom of the cabinet).

6.6.3 Use of repaired SSBs instead of new

Repaired SSBs on stock will obviously already contain main TV software. This implies that only a main software upgrade is required if you use a “repaired” SSB for board swap instead of a “new” SSB.

6.7 Total Overview SAM modes

Table 6-4 SAM mode overview

Main Menu	Sub-menu 1	Sub-menu 2	Sub-menu 3	Description
Hardware Info	A. SW VERSION	e.g. “Q5492_1.26.15.0”		Display TV & Standby SW version and CTN serial number.
	B. Standby processor version	e.g. “STDBY_88.68.0.0”		
	C. Production code	e.g. “See type plate”		
Operation hours				Displays the accumulated total of operation hours.TV switched “on/off” & every 0.5 hours is increase one
Error				Displayed the most recent errors.
Reset error buffer				Clears all content in the error buffer.
Alignment	Tuner AGC			RF-AGC Take over point adjustment (AGC default value is 80)
	Whitepoint	Colour temperature	Normal	3 different modes of colour temperature can be selected
			Warn	
			Cool	
		White point red		LCD White Point Alignment. For values, see Table 6-1 White D alignment values.
		White point green		
		White point blue		
		Red black level offset		
		Green black level offset		

Main Menu	Sub-menu 1	Sub-menu 2	Sub-menu 3	Description
Dealer options	Picture mute	Off/On		Select Picture mute On/Off. Picture is muted / not muted in case no input signal is detected at input connectors.
	Virgin mode	Off/On		Select Virgin mode On/Off. TV starts up / does not start up (once) with a language selection menu after the mains switch is turned “on” for the first time (virgin mode)
	E-sticker	Off/On		Select E-sticker On/Off (USP’s on-screen)
	Auto store mode	None		
		PDC/VPS		
		TXT page		
		PDC/VPS/TXT		
Options	Digital broadcast	DVB	Off/On	Select DVB On/Off
		DVB - T installation	Off/On or Country dependent	Select DVB T installation On/Off or by country
		DVB - T light	Off/On	Select DVB T light On/Off
		DVB - C	Off/On	Select DVB C On/Off
		DVB - C installation	Off/On or Country dependent	Select DVB C installation On/Off or by country
		Over the air download	Off/On or Country dependent	Select Over the air download On/Off or by country
		8 days EPG	Off/On	Select 8 day EPG On/Off
	Digital features	USB	Off/On	Select USB On/Off
		Ethernet	Off/On	Select Ethernet On/Off
		Wi-Fi	Off/On	Select Wi-Fi On/Off
		DLNA	Off/On	Select DLNA On/Off
		Online service	Off	Online service is Off
		PTP (Picture Transfer Protocol)	Off/On	Select PTP On/Off
		Update assistant	Off/On	Select Update assistant On/Off
		Internet software update	Off	Internet software update is Off
	Display	Screen	180 / LCD Sharp Z3LA13 56"	Displayed the panel code & type model.
		LightGuide	Off/On	Select LightGuide On/Off
		Display fans	Not present/Present	Select Display fans Present/Not present.
		Temperature sensor	Sensor present in display (only for 21:9)	N.A.
		Temperature LUT	0	N.A
		E-box & monitor	Off/On	Select E-box & monitor On/Off
	Video reproduction	Picture processing	None/PNX5100	Select Picture processing None/PNX5100 (Q549.xE chassis).
		MOP local contrast	Off/On	Select MOP local contrast On/Off
		Light sensor	Off/On	Select Light sensor On/Off
		Light sensor type	0/1/2/3	Select Light sensor type form 0 to 3 (for difference styling).
		Pixel Plus type	Pixel Plus HD	Select type of picture improvement.
			Perfect Pixel HD	
			Pixel Precise HD	
		Ambilight	None,	Select type of Ambilight modules use.
			2 sided 2/2	For 8400 series only
			2 sided 4/4	
			3 sided 2/3/2	
			3 sided 4/3/4	
			3 sided 4/5/4	
			4 sided 4/3/4/3	
		Ambilight technology	LED/Future use	Ambilight technology LED is in use.
		MOP ambilight	Off/On	Select MOP ambilight On/Off

Main Menu	Sub-menu 1	Sub-menu 2	Sub-menu 3	Description
	Audio reproduction	Acoustic system		Cabinet design used for setting dynamic audio parameters.
	Source selection	EXT1/AV1 type	SCART CVBS RGB LR	Select input source when connected with external equipment.
			CVBS Y/C YPbPr LR	
			CVBS Y/C YPbPr HV LR	
			(CVBS) YPbPr LR	
		EXT2/AV2 type	SCART CVBS RGB LR	Select input source when connected with external equipment.
			CVBS Y/C LR	
			(CVBS) YPbPr LR	
			CVBS Y/C LR	
		EXT3/AV3 type	None	Select input source when connected with external equipment.
			CVBS	
			CVBS LR	
			YPbPr	
			YPbPr LR	
			YPbPr HV LR	
		VGA	Off/On	Select VGA On/Off
		SIDE I/O	Off/On	Select SIDE I/O On/Off
		HDMI 1	Off/On	Select HDMI 1 On/Off
		HDMI 2	Off/On	Select HDMI 2 On/Off
		HDMI 3	Off/On	Select HDMI 3 On/Off
		HDMI 4	Off/On	Select HDMI 4 On/Off
		HDMI side	Off/On	Select HDMI side On/Off
		HDMI CEC	Off/On	Select HDMI CEC On/Off
		HDMI CEC RC passthrough	Off/On	Select HDMI CEC RC passthrough On/Off
		HDMI CEC Pixel Plus link	Off/On	Select Pixel Plus link On/Off
	Miscellaneous	Region	Europe/AP-PAL-MULTI/Australia	Select Region/country.
		Tuner type	HD1816-MK1/TD1716-MK4/ TD1716-MK3/HD1816-MK2	Select type of Tuner used.
		System RC support	Off/On	Select System RC support On/Off.
		Embedded user manual	Off/On	Select Embedded user manual On/Off.
		Start-up screen	Off/On	Select Start-up screen On/Off.
		Wallpaper	Off/On	Select Wallpaper On/Off.
		Hotel mode	Off	Hotel mode is Off.
Option number	Group 1	e.g. “08192.02181.01387.45160”		The first line (group 1) indicates hardware options 1 to 4.
	Group 2	e.g. “10185.12448.00164.00000”		The second line (group 2) indicates software options 5 to 8.
	Store			Store after changing.
Initialise NVM				N.A
Store				Select Store in the SAM root menu after making **any** changes.
Software maintenance	Software events	Display		Display information is for development purposes.
		Clear		
		Test reboot		
	Hardware events	Display		Display information is for development purposes.
		Clear		
Operation hours display		0003		In case the display must be swapped for repair, you can reset the ""Display operation hours"" to ""0"". So, this one does keeps up the lifetime of the display itself (mainly to compensate the degeneration behaviour).
Test setting	Digital info	QAM modulation: 64-QAM		Display information is for development purposes.
		Symbol rate: 23:29		
		Original network ID: 12817		
		Network ID:12817		
		Transportstream ID: 2		
		Service ID: 3		
		Hierarchical modulation: 0		
		Selected video PID: 35		
		Selected main audio PID: 99		
		Selected 2nd audio PID: -1		
	Install start frequency	000		Install start frequency from "0" MHz
	Install end frequency	999		Install end frequency as 999 MHz
	Default install frequency			
	Installation	Digital only		Select Digital only or Digital + Analogue before installation.
		Digital + Analogue		

Main Menu	Sub-menu 1	Sub-menu 2	Sub-menu 3	Description
Development file versions	Development 1 file version	Display parameters DISPT 3.26.8.7		Display information is for development purposes.
		Acoustics parameters ACSTS 3.6.6.5		
		PQ - PRFPP 1.26.10.4		
		Ambilight parameters PRFAM 2.6.1.3		
	Development 2 file version	12NC one zip software		Display information is for development purposes.
		Initial main software		
		NVM version Q5492_0.4.0.0		
		Flash units SW Q5492_0.26.15.0		
Upload to USB	Channel list			To upload several settings from the TV to an USB stick
	Personal settings			
	Option codes			
	Display-related alignment			
	History list			
Download from USB	Channel list			To download several settings from the USB stick to the TV.
	Personal settings			
	Option codes			
	Display-related alignment			

7. Circuit Descriptions

Index of this chapter:

Notes:

- Only **new** circuits (circuits that are not published recently) are described.
- Figures can deviate slightly from the actual situation, due to different set executions.
- For a good understanding of the following circuit descriptions, please use the wiring, block (see chapter 9. Block Diagrams) and circuit diagrams (see chapter 10. Circuit Diagrams and PWB Layouts).Where necessary, you will find a separate drawing for clarification.

7.1 Introduction

The Q549.2E LA chassis (platform name TV543/92) is the successor of the Q529.1E LA chassis (platform TV522/92).

Main difference with the previous platform is the introduction of “Net TV” and “CI+”.

7.1.1 Implementation

Key components of this chassis are:

- PNX8543 Digital Colour Decoder
- EP3C25F324C7N FPGA (“Local Contrast”)
- HD1816AF Hybrid Tuner
- DRX3926K Demodulator
- TDA9996 HDMI Switch
- TPA3123D2PWP Class D Power Amplifier
- DP83816AVNG PCI ethernet media access controller and physical layer (MacPhyter-II).

7.1.2 TV543 Architecture Overview

- For details about the chassis block diagrams refer to chapter 9. Block Diagrams. An overview of the TV543 architecture can be found in Figure 7-1.

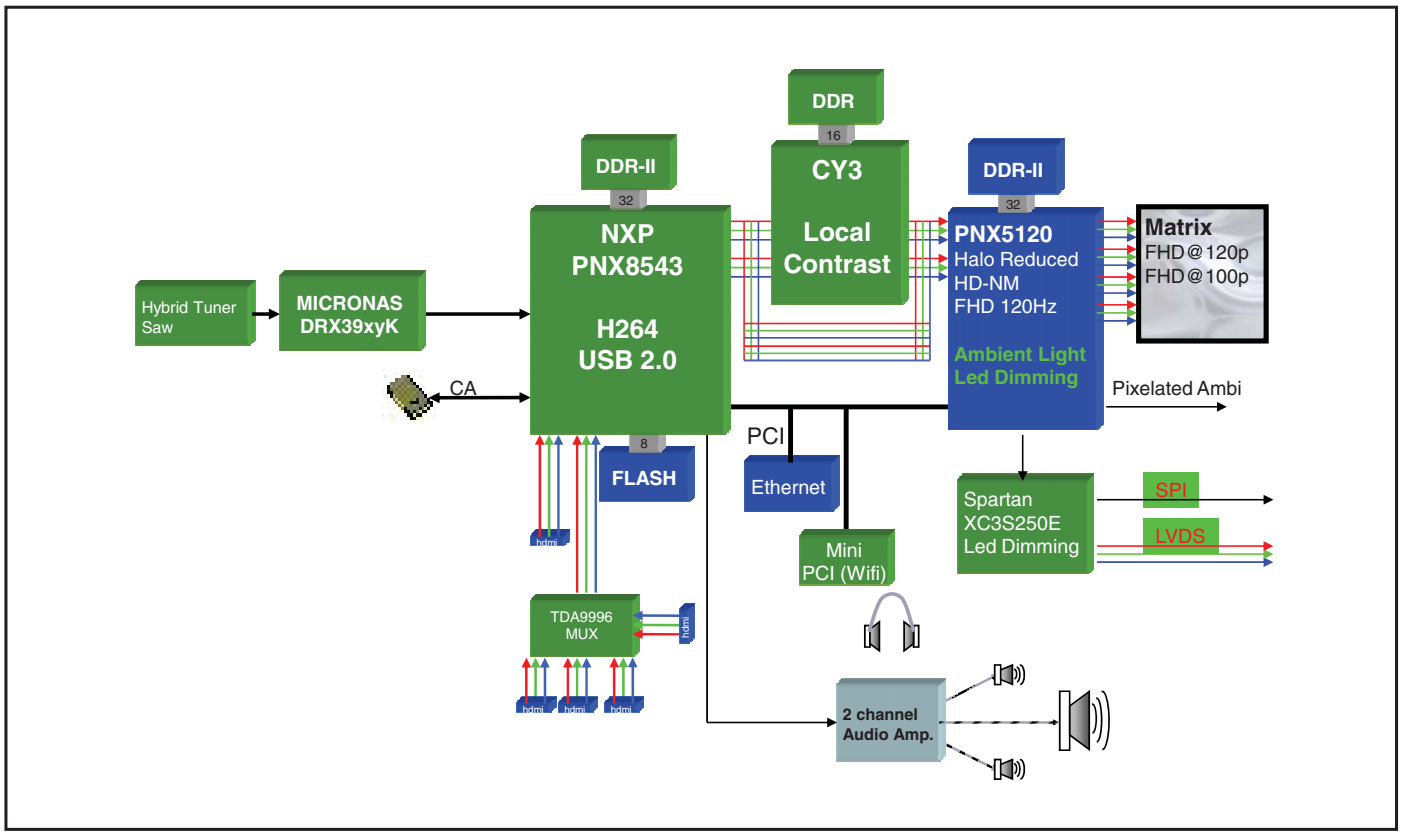

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Figure 7-1 Architecture of TV543/92 Elite Core platform

7.1.3 SSB Cell Layout

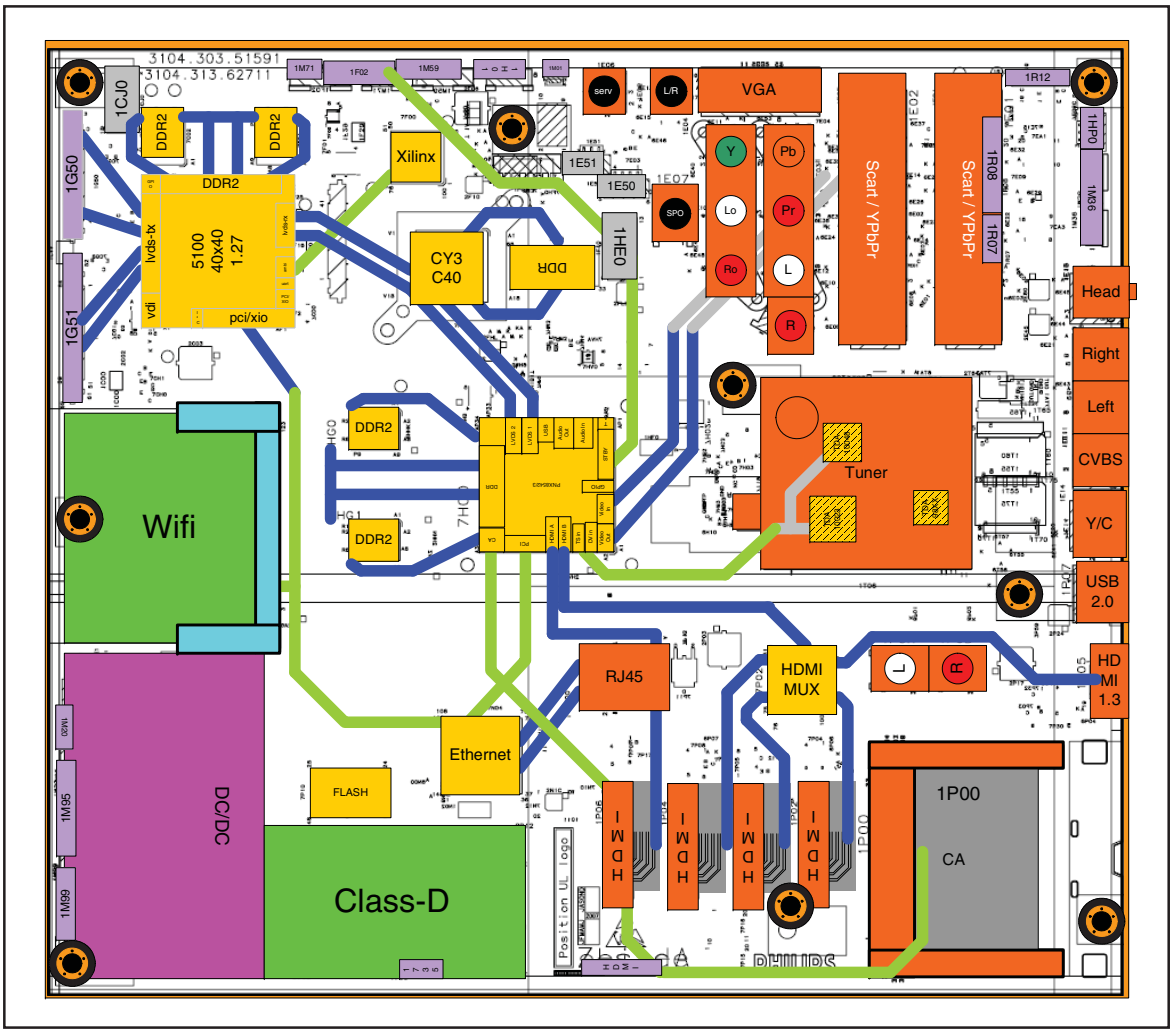

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Figure 7-2 SSB layout cells (top view)

7.2 Power Architecture

Refer to figure Figure 7-3 for the power architecture of this platform.

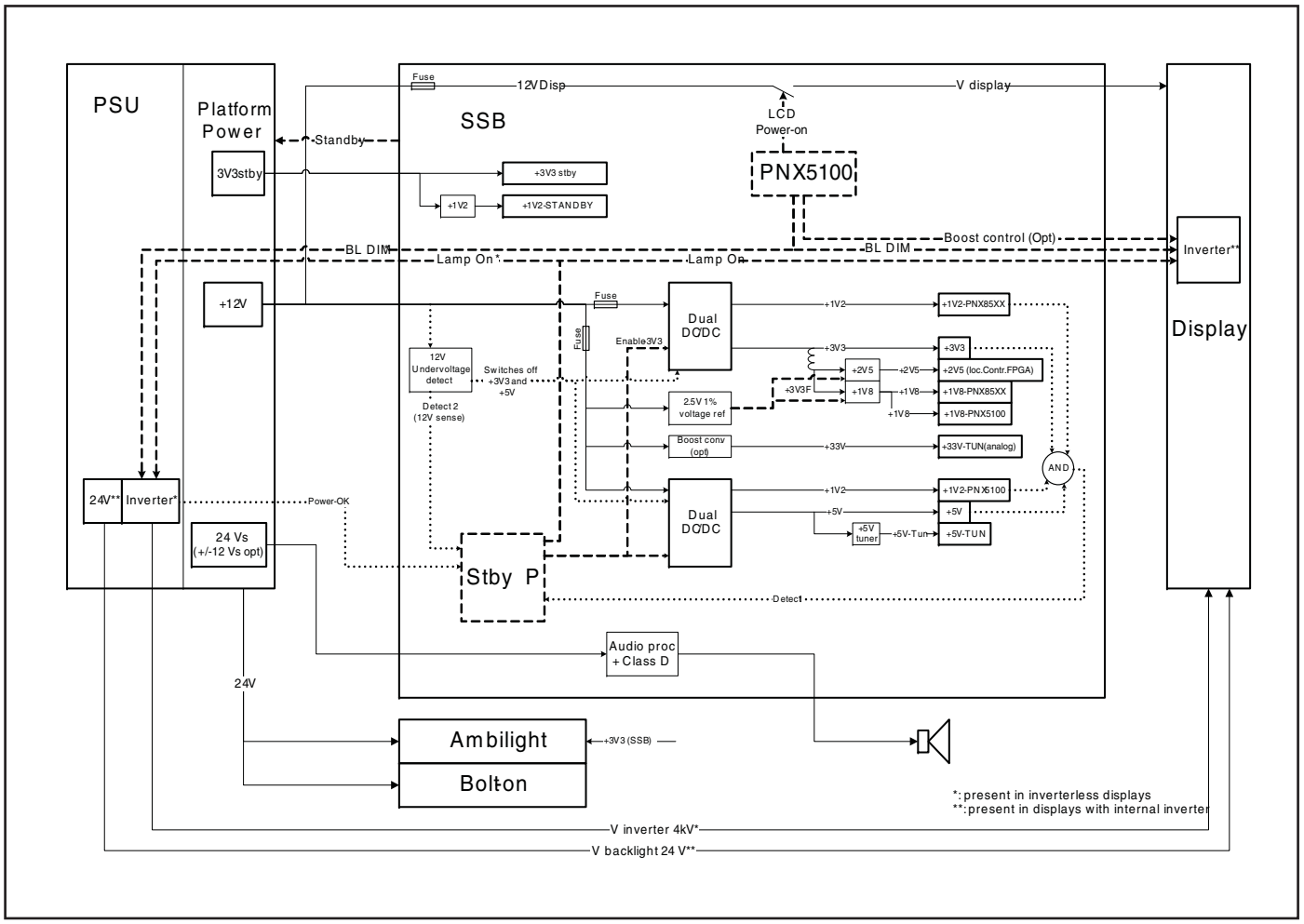

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Figure 7-3 Power Architecture TV543/92 platform

7.2.1 Power Supply Unit

All power supplies are a black box for Service. When defective, a new board must be ordered and the defective one must be returned, unless the main fuse of the board is broken. Always replace a defective fuse with one with the correct specifications! This part is available in the regular market. Consult the Service website for the order codes of the boards.

In the TV543 Elite Core platform, for sets up to and including 47", the Integrated Power Board (IPB) - incl. inverter is used. For sets of 52 " and 56", a conventional PSU (with additional inverters) is used.

In this manual, no detailed information is available because of design protection issues.

The output voltages to the chassis are:
- +3V3-STANDBY (standby-mode only)
- +12V (on-mode)
- +Vsnd (+24V) (audio power) (on-mode)
- +24V (bolt-on power) (on-mode)
- IPB: High voltage to the LCD panel (for sets up to and including 47").

7.2.2 Diversity

Below find an overview of the different PSUs that are used:

Table 7-1 Supply diversity

Supplier	PSU	Model	Input Voltage Range
LGIT	PLHL-T826A	32"	High Mains (198- 265 Vac)
Delta	DPS-298CP A	37"	High Mains (198- 265 Vac)
Delta	DPS-411AP-3 A	56"	High Mains (198- 265 Vac)

7.3 Front-End

The Front-End consist of the following key components:

- Tuner HD1816AF
- SAW filter 36M125
- IF demodulator DRX3926K
- AGC amplifier UPC3221GV.

Below find a block diagram of the front-end application.

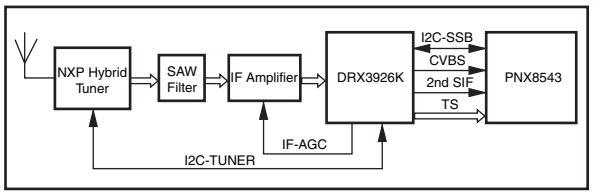

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Figure 7-4 Front-End block diagram

The DRX3926K is a multi-standard demodulator supporting DVB-C, DVB-T and analogue standards. The demodulated digital stream is fed into the parallel transport stream data ports of the PNX8543. The demodulated analogue signal in the form of CVBS is connected to the analogue video CVBS/Y input channel, while the SIF is connected via the SSIF2 positive input port.

7.4 HDMI

In this platform, the TDA9996 HDMI multiplexer is implemented. Only for one HDMI input, a separate EEPROM is implemented to store the EDID values. For the other HDMI inputs, the EDID contents are no longer stored in a separate EEPROM, but directly in the multiplexer. Each input has its own physical subaddress: the first 253 bytes are common, where the last 3 bytes define the specific input. The EDID contents are, at +5V power-up, downloaded to RAM. The following figures show the HDMI input configuration and EDID control.

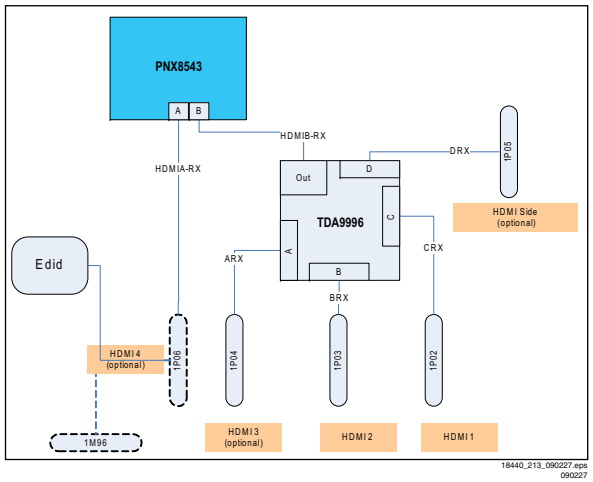

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Figure 7-5 HDMI input configuration

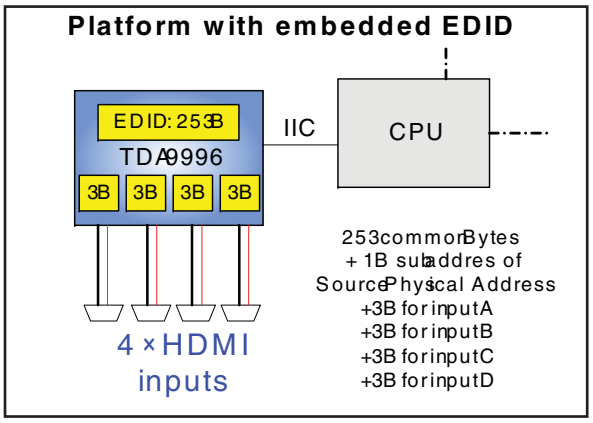

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Figure 7-6 EDID control (embedded EDID)

The delta's with respect to the use of the TDA9996 as HDMI multiplexer compared with earlier chassis/platforms are:

- +5V detection mechanism
- Stable clock detection mechanism
- Integrated EDID
- RT control
- HPD control
- TMDS output control
- CEC control
- New hotplug control for PNX8543 for 5th HDMI input
- New EDID structure: EDID stored in TDA9996, therefore there are no EDID pins on the SSB. Only in the event of a 5th HDMI input, an additional EEPROM is foreseen, as was implemented in previous platforms.

After replacement of the TDA9996 HDMI mux, the default I^2C address should be reprogrammed from C0 to CE, and the HDMI EDIDs should be reprogrammed as well. Both actions should be executed via ComPair.

7.5 Video and Audio Processing - PNX8543

The PNX8543 is the main audio and video processor (or System-on-Chip) for this platform. It is a member of the PNX85xx SoC family (described in earlier chassis) with the addition of the MPEG4 functionality; the separate STi710x MPEG4 decoder is no longer implemented in this platform.

Some more delta's compared to the previous PNX85xx are:

- 2 HDMI inputs (A & B)
- HDMI deep colour RGB/YCbCr 4:4:1 10/12 bit detection.

The PNX8543 handles the digital and analogue audio- and video decoding and processing. The processor is a MIPS32 general purpose CPU and a 8051-based TV controller for power management and user event handling.

- For a functional diagram of the PNX8543, refer to Figure 7-7.

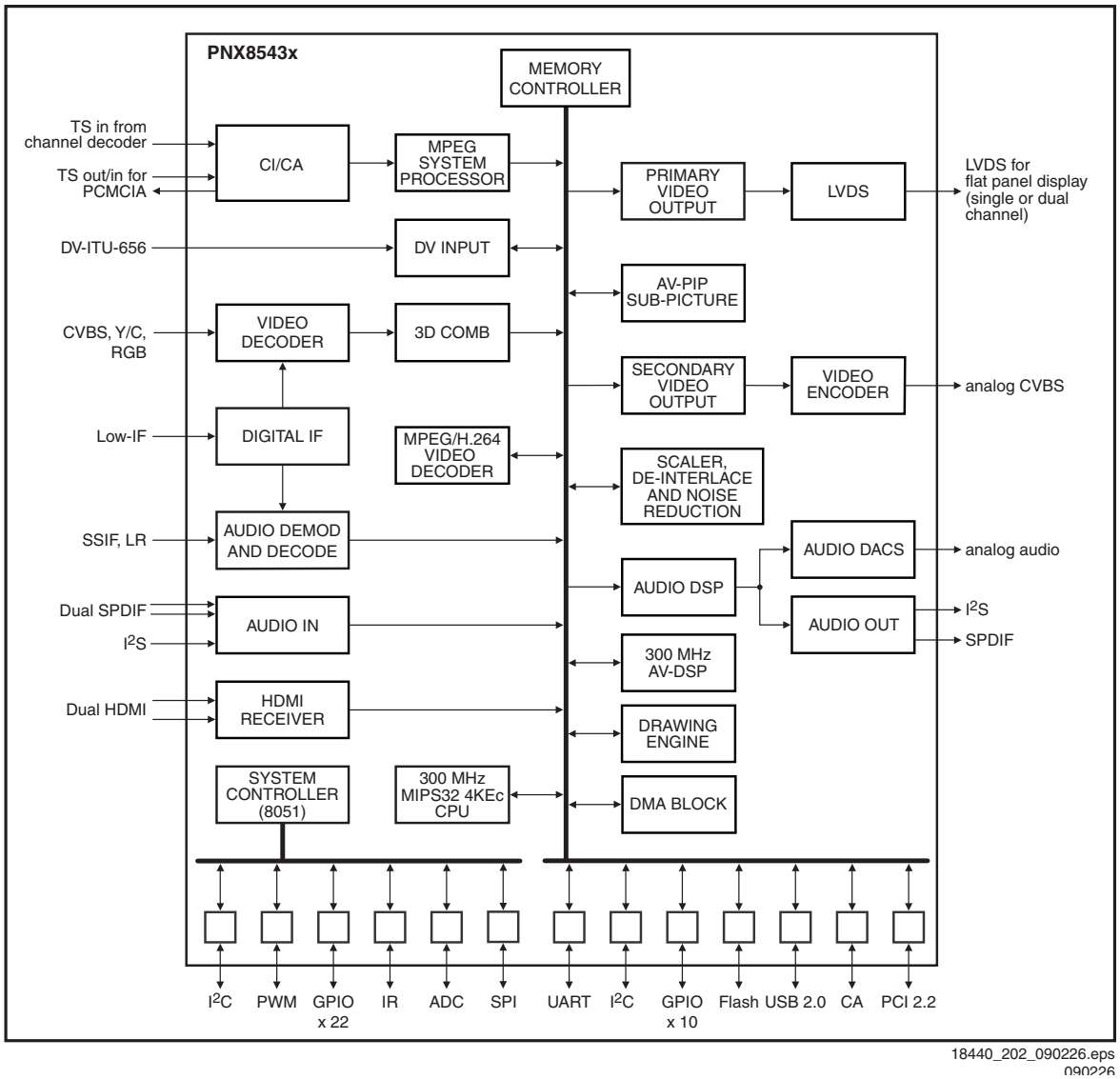

Figure 7-7 PNX8543 functional diagram

7.5.1 Video Subsystem

Refer to Figure 7-8 for the main video interfaces for the PNX8543 and the video signal flow between blocks and memory.

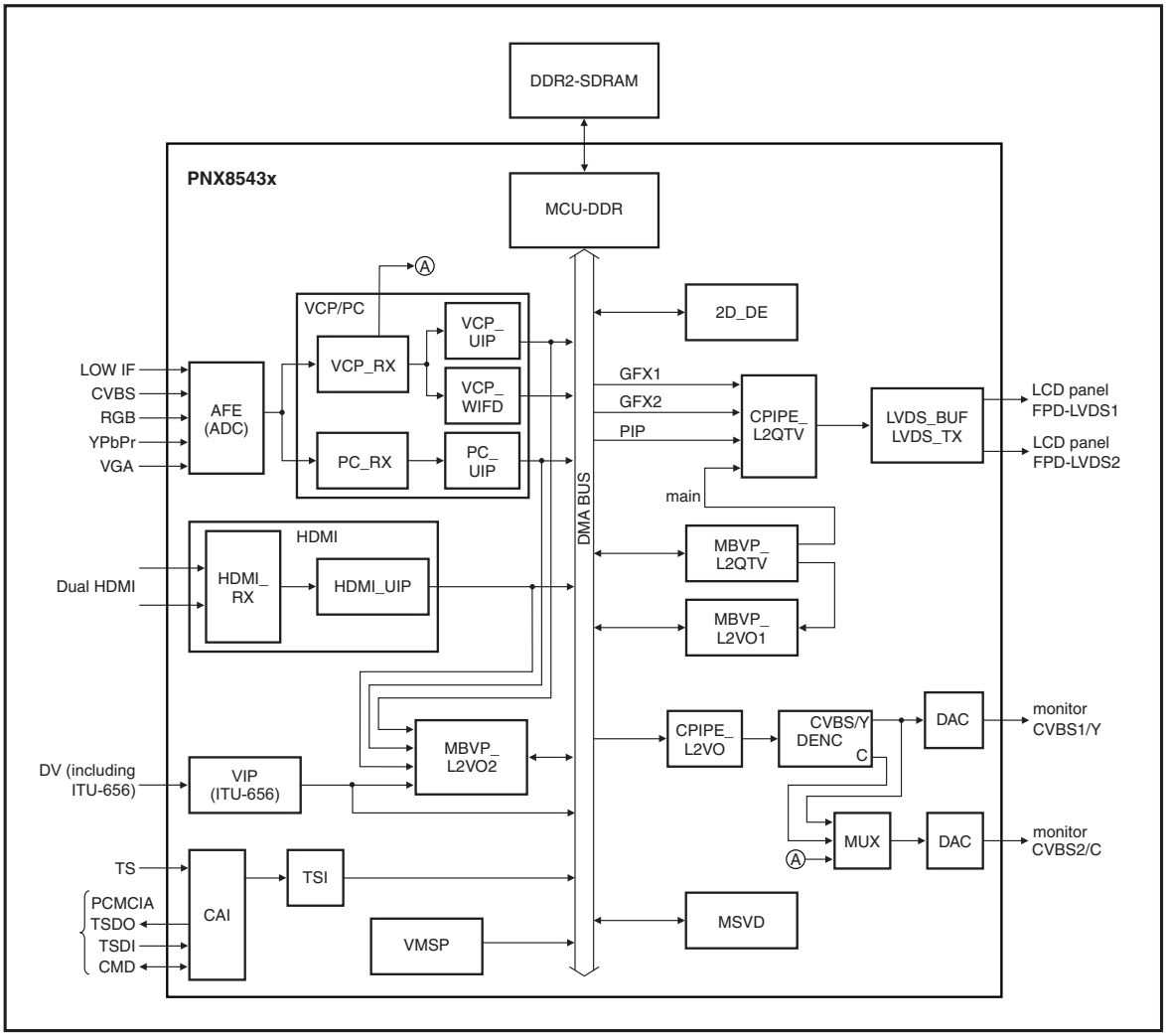

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Figure 7-8 PNX8543 video flow diagram

The Video Subsystem consist of the following blocks:

- Analogue Front-End (AFE) block
- Video and PC Capture (VPC/PC) pipe
- HDMI Receiver interface
- Memory-Based Video Processor MBVP)
- Video Composition Pipe (CPIPE)
- Memory Based Video Processor (MBVP) VO-1
- Memory Based Video Processor (MBVP) VO-2
- Video Composition Pipe (CPIPE)
- Dual Flat Panel Display-LVDS (FPD-LVDS)
- Digital Encoder (DENC)
- Digital Video VIP
- 2D graphics block.

7.5.2 Audio Subsystem

Refer to Figure 7-9 for the main audio interfaces for the PNX8543 and the audio signal flow between blocks and memory.

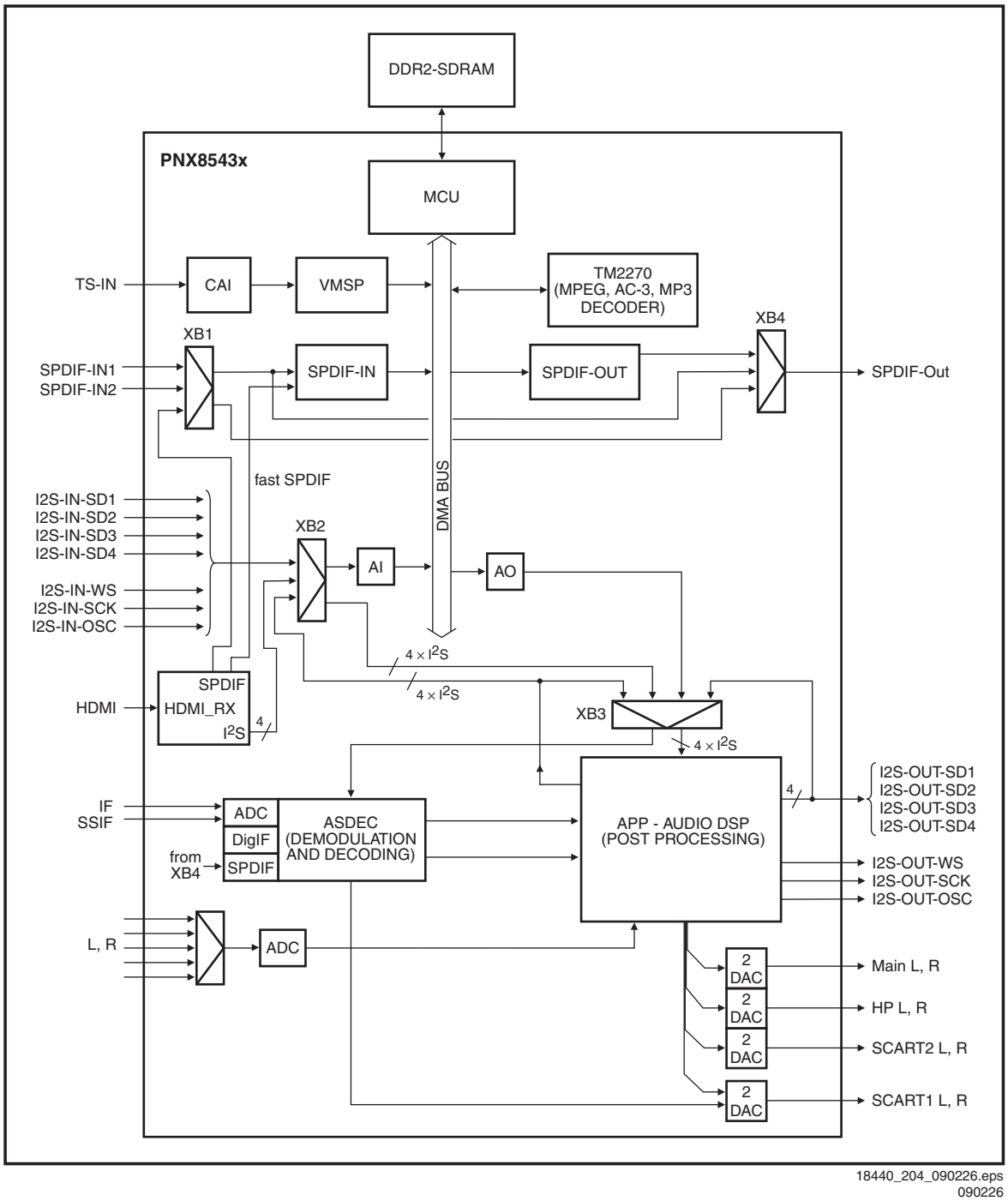

Figure 7-9 PNX8543 audio flow diagram

The Audio Subsystem consist of the following blocks:

- Analogue Audio Front End (AAFE) used to capture Baseband Audio Inputs and to sample Secondary Sound IF (SSIF) directly or via Low-IF input
- HDMI Receiver interface block
- SPDIF input block
- Audio Input (AI) block
- Audio Output (AO) block
- Demodulation & Decoding (ASDEC) DSP for decoding all analogue terrestrial TV sound standards
- Audio Post-Processing (APP) block
- Digital Audio decoder.

7.5.3 Connectivity and Compute Subsystem

Refer to Figure 7-10 for the connectivity and compute subsystem.

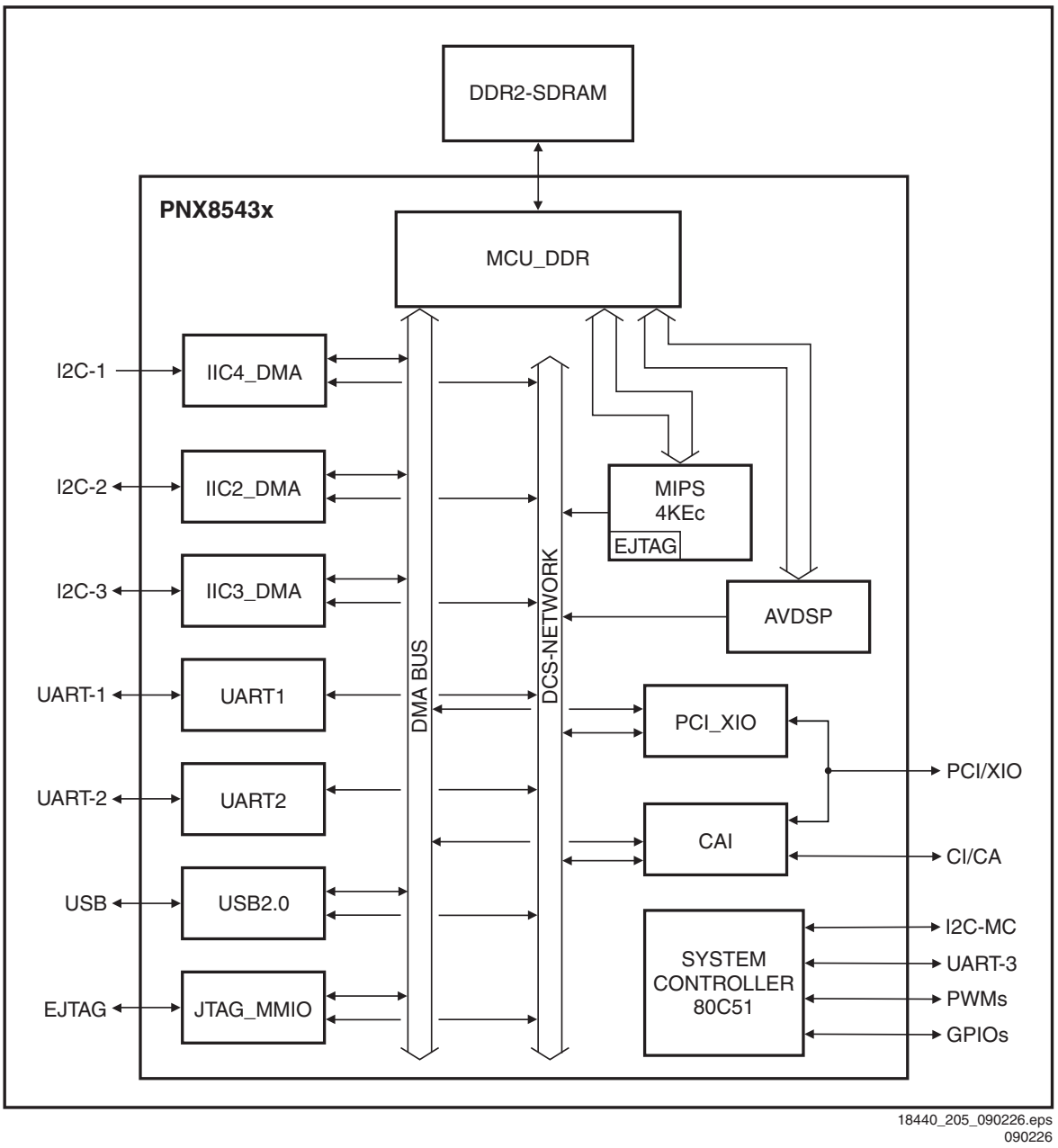

Figure 7-10 PNX8543 connectivity and compute subsystem

The Connectivity Subsystem consists of:
- PCI/XIO interface
- USB2.0 interface
- Three 2-wire UARTs
- Four Master/Slave I^2C interfaces
- Common Interface/Conditional Access Interface.

The Computing Subsystem consists of:
- 32-bit MIPS RISC core
- Enhanced JTAG (EJTAG) block inside the MIPS
- JTAG_MMIO blocks
- TV controller
- Audio/Video DSP (AV_DSP)
- Memory Control Unit (MCU).

7.5.4 Service Notice - FLASH RAM / PNX8543 exchange

The FLASH RAM (item 7P10) and/or PNX8543 (item 7H00) can only be exchanged by an authorised central workshop with dedicated programming tools. Due to the presence of (CI+) keys in the components, **unauthorised exchange of these components will always result in a defective board**.

7.6 Common Interface CI+

Together with this platform, an extention to the Common Interface (CI) Conditional Access system is added, called CI+.

CI+ or Common Interface Plus is a specification that extends the Common Interface (DVB-CI) as described in the digital broadcasting standard DVB.

The weakness of the conventional CI module as Conditional Access system was the absence of a Copy Protection mechanism, as decrypted content could be sent over the PCMCIA interface unscrambled. With the CI+ extension, a form of copy protection is established between the Conditional Access Module (CAM) and the Integrated Digital Television (IDTV). The security mechanisms in CI+ are derived/copied from POD (with the exception of Out Of Band (OOB) used in US CA systems). For more information about conventional CA systems using a CI module, refer to the BJ3.0E L/PA or BL2.xU Service Manual.

The CI+ standard is downwards compatible with the existing CI standard.

The following figure shows the implementation of the CI+ Conditional Access system in the TV543 platform.

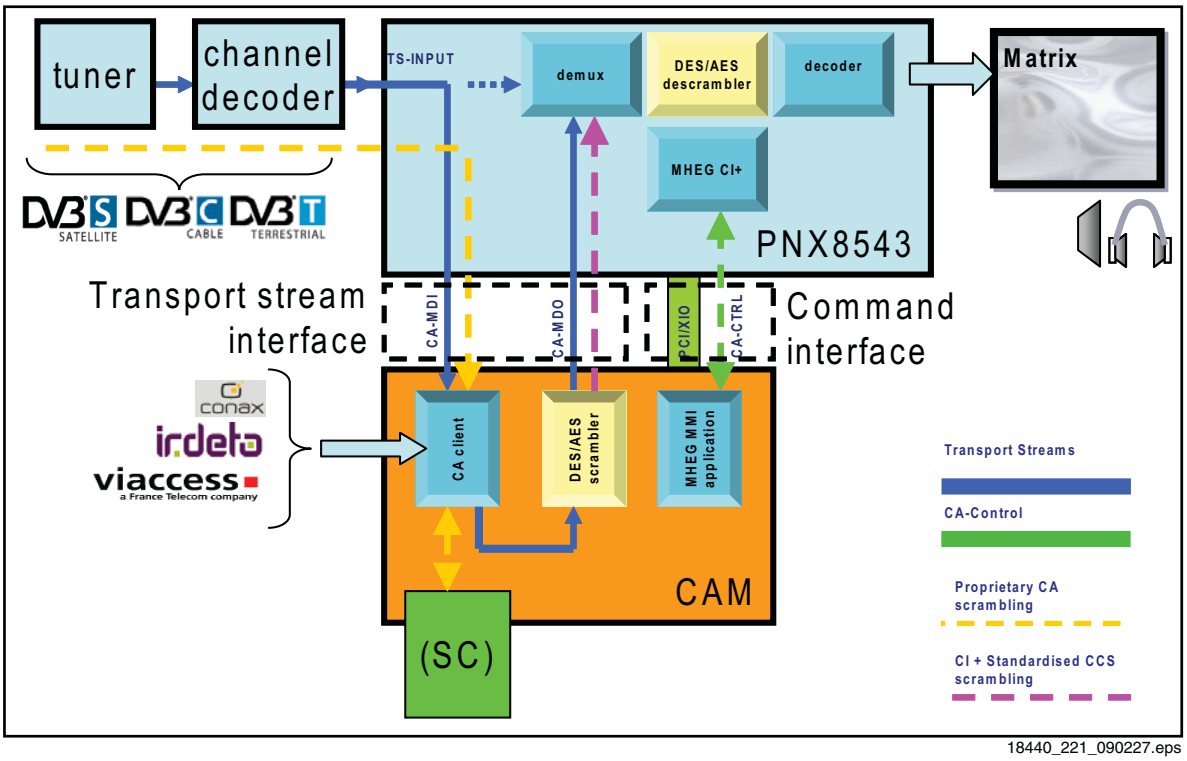

Figure 7-11 CI+ Conditional Access implementation

7.7 Net TV

In this chassis, a feature that enables access to dedicated internet pages from a limited group of information suppliers, called “Net TV”, is introduced. A separate Wi-Fi module enables wireless communication with a local network.

7.8 Ambi Light

The Ambi Light architecture in this platform has been entirely renewed. The characteristics are:

- Additional DC/DC board generating 12/16/24 V (optional)
- ARM processor (on DC/DC panel or AL board)
- Low-power LEDs
- SPI interface from ARM to LED drivers
- I^2C upgradeable via USB
- Each AL module has a temperature sensor.

The use of the DC/DC board is optional. In case no DC/DC board is implemented, the ARM processor is located on one of the AL boards.

Refer to Figure 7-12 for the Ambi Light architecture.

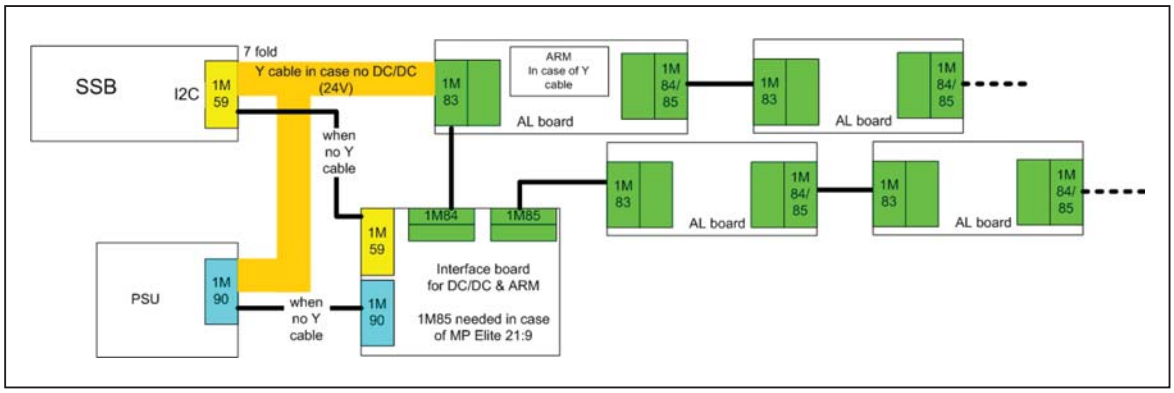

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Figure 7-12 Interface between Ambi Light and SSB

7.8.1 ARM controller

Refer to Figure 7-13 below for signal interfacing to and from the ARM controller. The ARM controller is located on the DC/DC board (item no. 7302) or AL panel (item no. 7102).

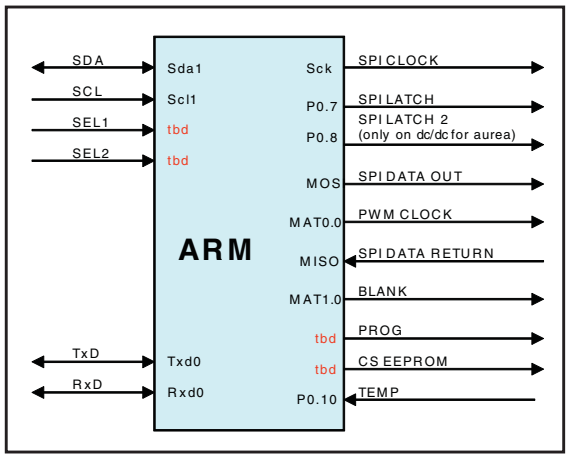

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Figure 7-13 ARM controller interface

Data transfer between ARM processor and LED drivers is executed by a Serial Peripheral Interface (SPI) bus interface.

The SPI bus is a synchronous serial data link standard that operates in full duplex mode.

For debugging purposes, the working principle is given below:

- At startup the controller will read-out matrix data from the EEPROM devices (via SPI DATA RETURN)
- Before operation, the driver current is set via SPI, with driver in DC mode
- During normal operation the controller receives RGB-, configuration-, operation mode- and topology data via I^2C
- The controller converts the I^2C RGB data via the matrixes to SPI LED data
- Via data return the controller receives error data (if applicable).

Also PWM clock and BLANK signals are generated by the controller. The controller can be reprogrammed via I^2C (via USB). The controller can receive matrix values via I^2C, which will be stored in the EEPROM of each AL module via the SPI bus. The temperature sensor in each AL module controls the TEMP line; in case of a too high temperature the controller will reduce the overall brightness.

7.8.2 LED driver communication (via SPI bus)

Refer to Figure 7-14 below for signal interfacing between the ARM controller and the LED drivers on the AL boards, and the LED drivers and the EEPROMs on the AL boards.

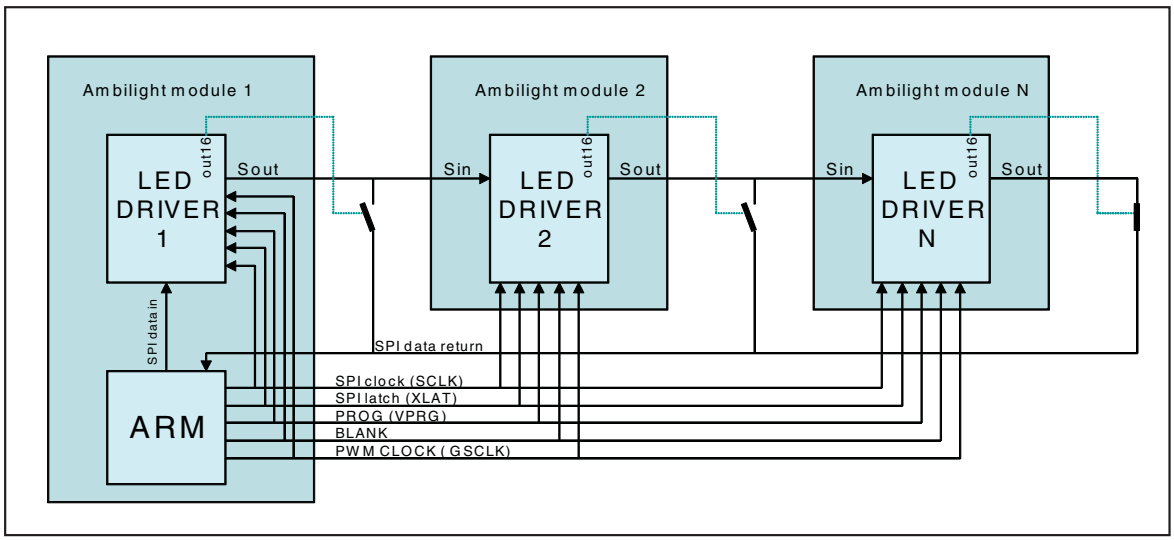

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Figure 7-14 SPI communication between ARM controller and LED drivers

The ARM controller communicates with the LED drivers (on each AL module) via an SPI bus. For debugging purposes, the working principle is given below:

- Data from the ARM controller is linked through the drivers, which are connected in cascade
- SPI CLK, SPI LATCH, PROG, BLANK and PWM CLOCK are going directly from the controller to each driver
- SPI DATA RETURN is linked from the last driver to the controller: controller decides which driver returns data.

7.8.3 Temperature Control

Refer to Figure 7-15 for signal interfacing between the ARM controller and the temperature sensor on the AL boards.

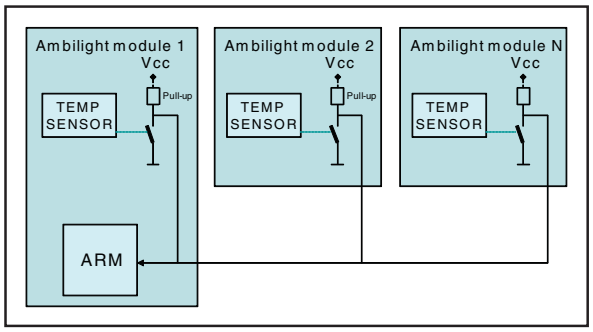

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Figure 7-15 Communication between ARM controller and temperature sensor

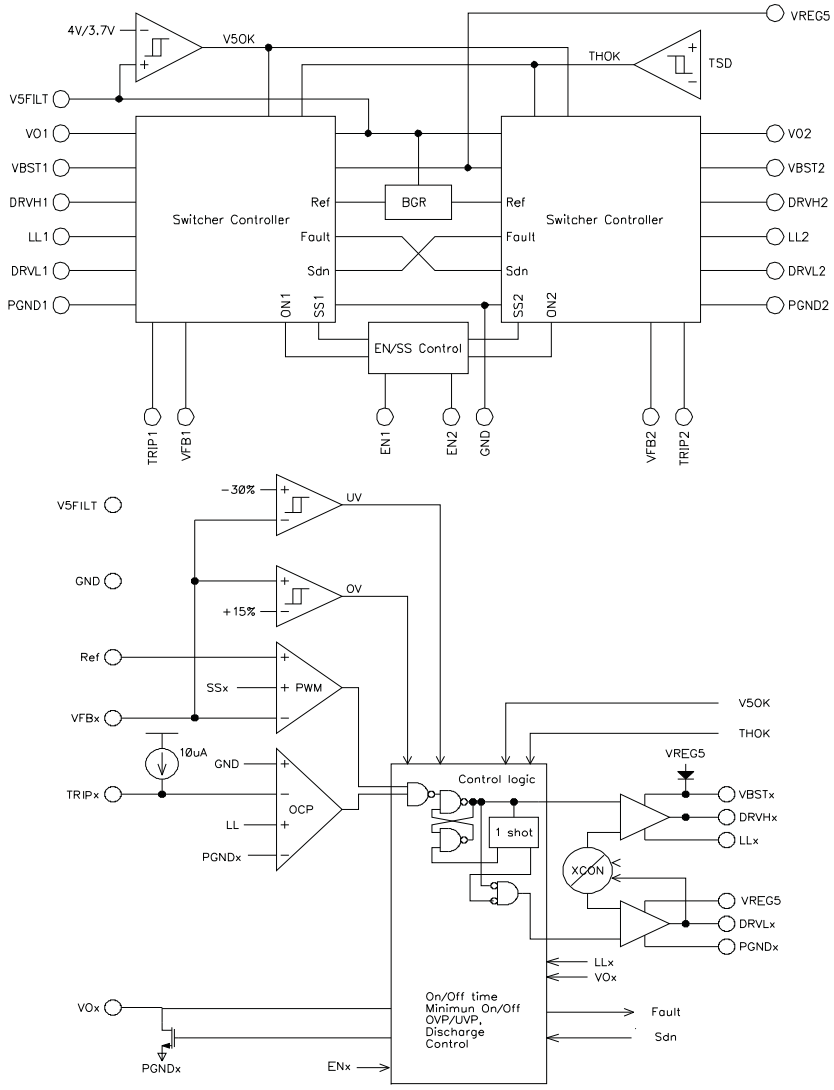
Each AL board is equipped with a temperature sensor. If one of the sensors detects a temperature over the threshold, the TEMP line is pulled LOW which results in brightness reduction.

8. IC Data Sheets

This chapter shows the internal block diagrams and pin configurations of ICs that are drawn as “black boxes” in the electrical diagrams (with the exception of “memory” and “logic” ICs).

8.1 Diagram SSB: DC/DC B01A, TPS53124PW (IC 7U03)

Block Diagram



Pin Configuration

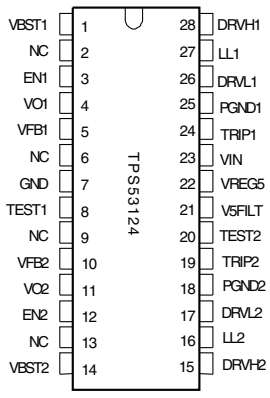


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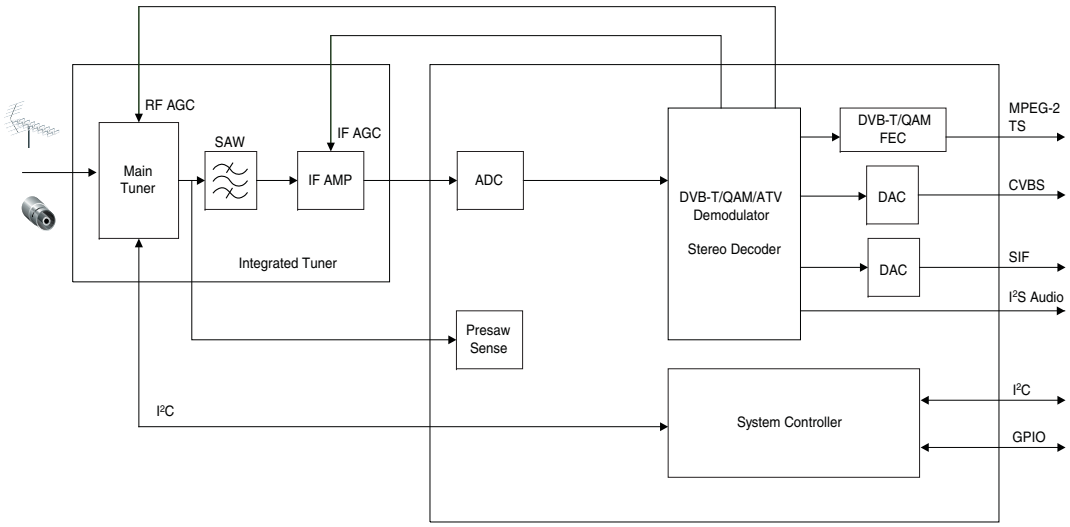
Figure 8-1 Internal block diagram and pin configuration

8.2 Diagram SSB: Front End B02B, DRX3926K (IC 7T50)

Block Diagram



Pin Configuration

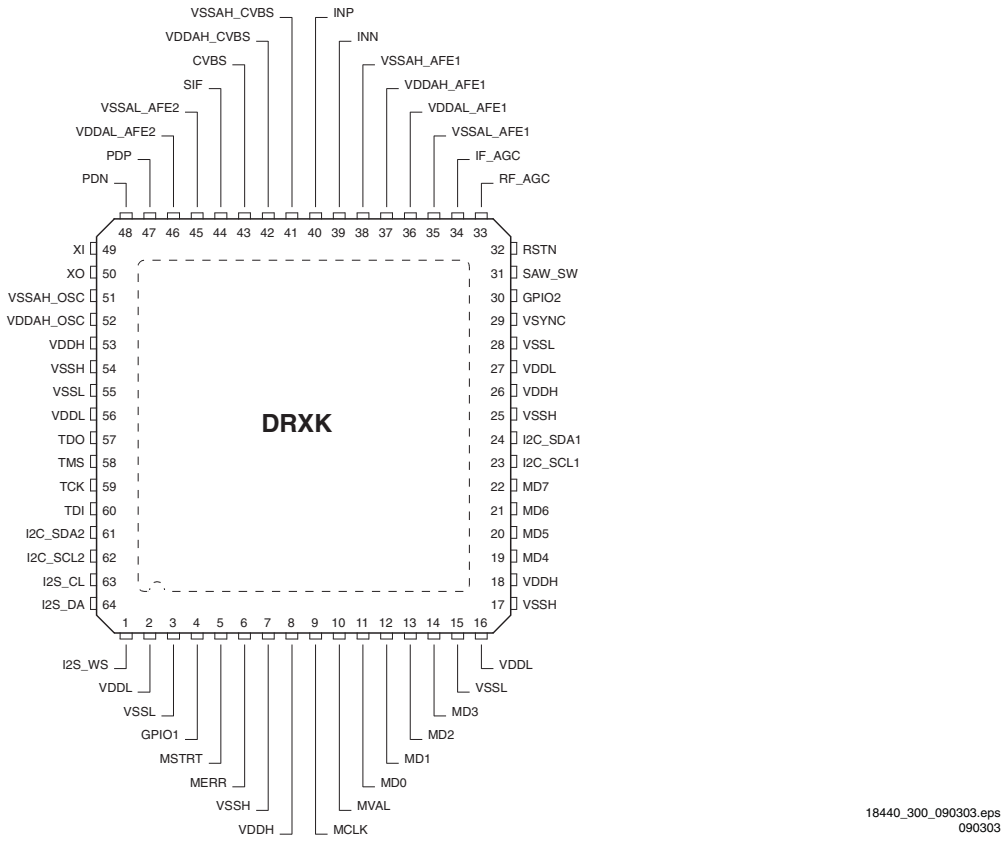
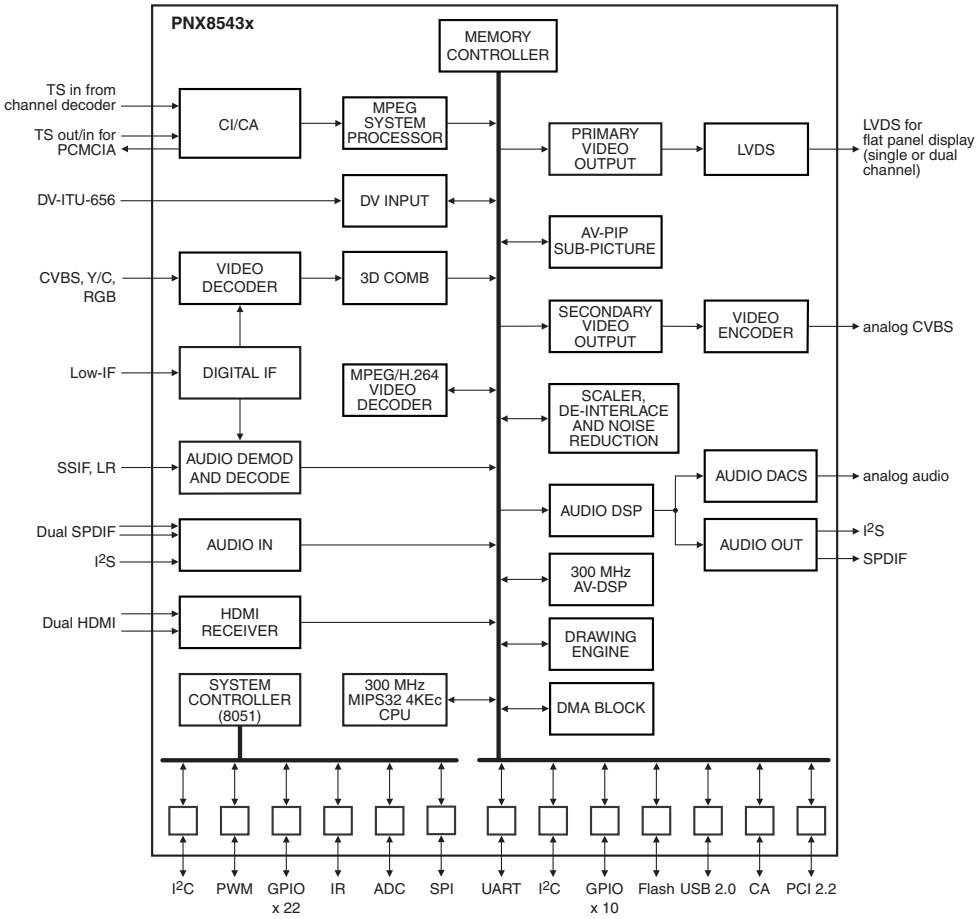


Figure 8-2 Pin configuration

8.3 Diagram SSB: PNX8543 - Stand-by Controller B04A, PNX8543 (IC7H00)

Block Diagram



Pin Configuration

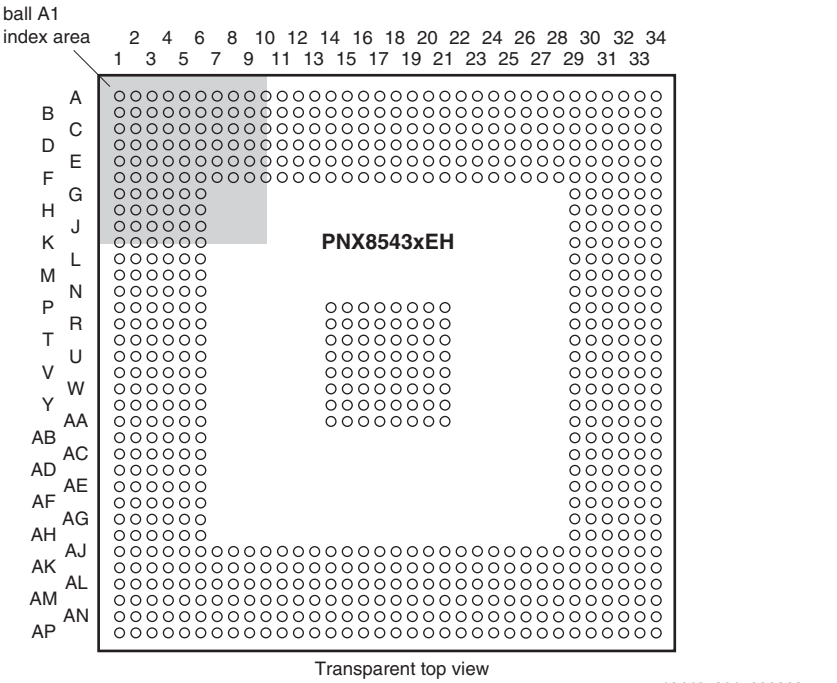


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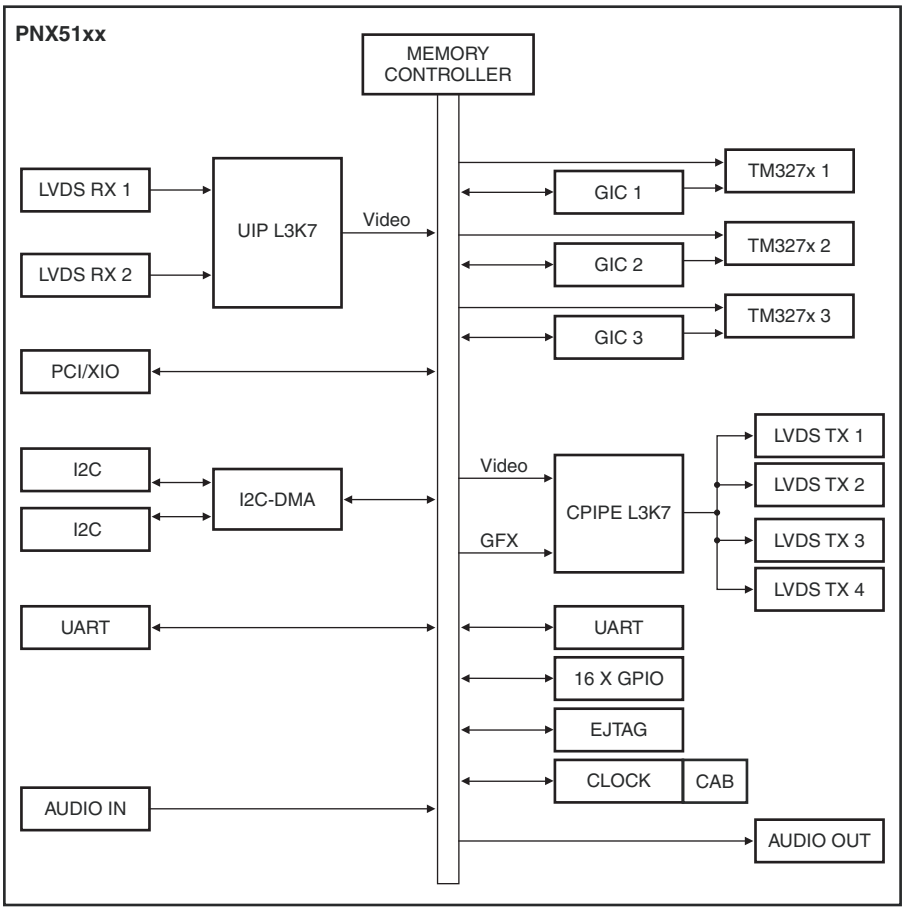
Figure 8-3 Internal block diagram and pin configuration

8.4 Diagram SSB: Ethernet B05A, PNX5120 (IC7C00)

Block Diagram



Pin Configuration

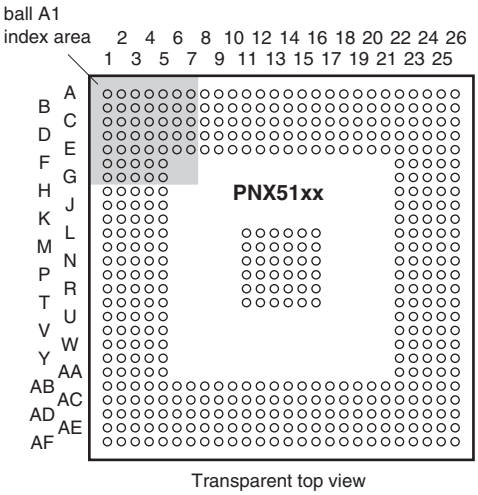


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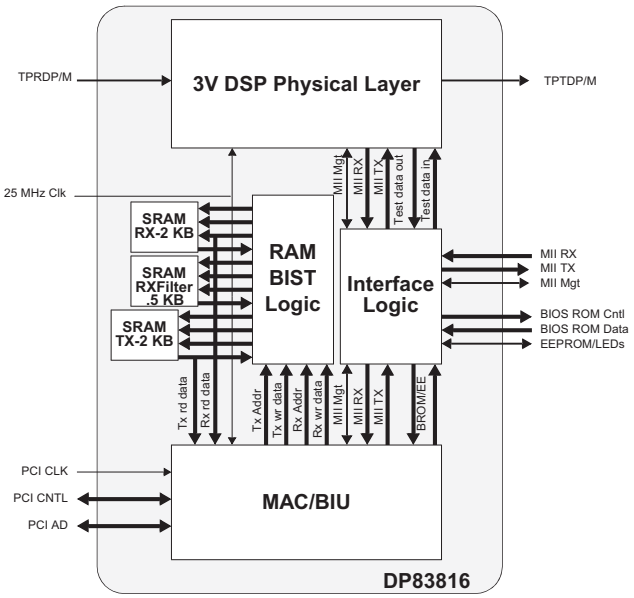
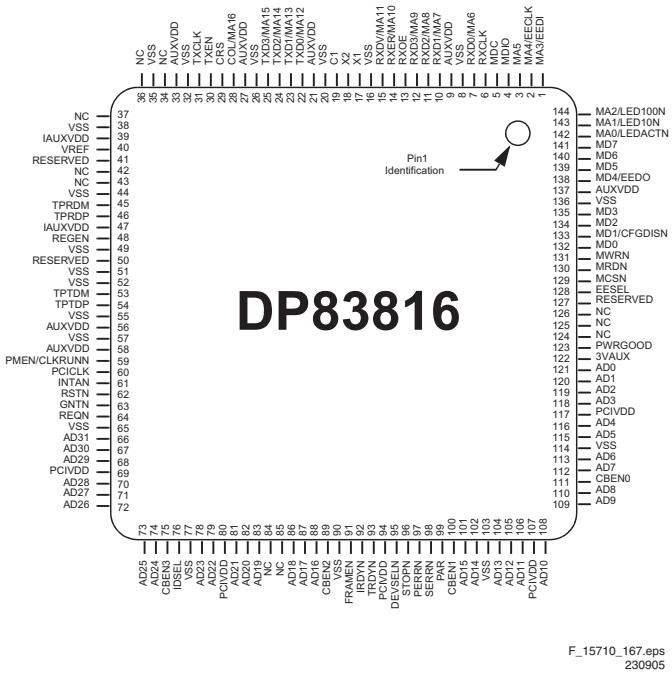
Figure 8-4 Internal block diagram and pin configuration

8.5 Diagram SSB: Ethernet B07G, DP83816 (IC7N04)

Block Diagram



Pin Configuration



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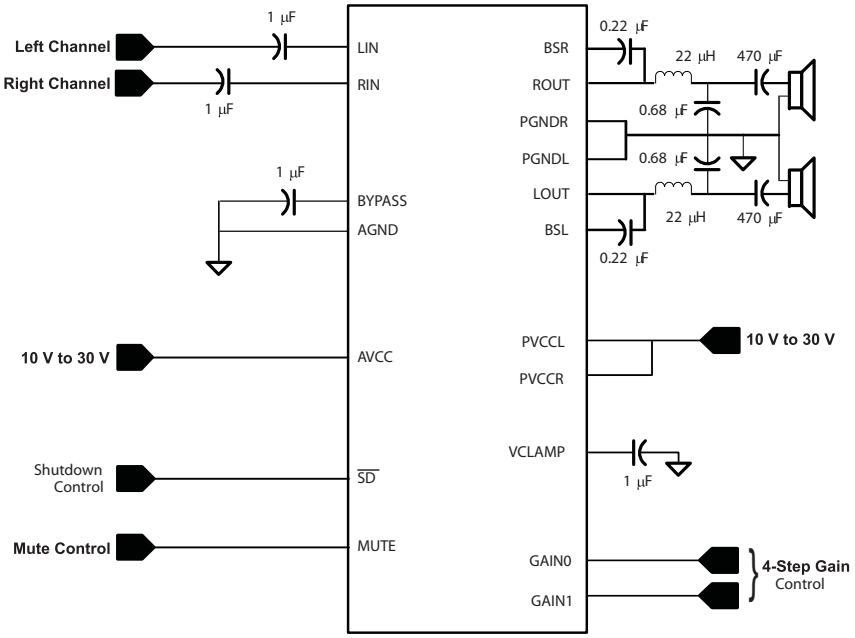
230905

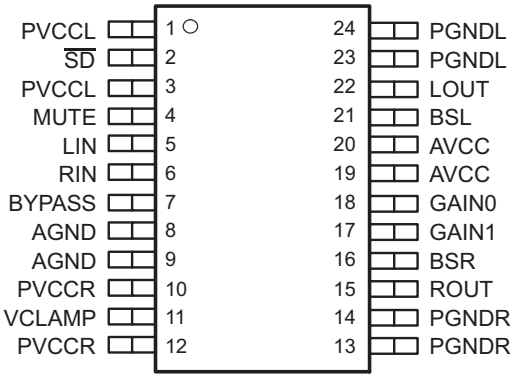
Figure 8-5 Internal block diagram and pin configuration

8.6 Diagram SSB: Audio B10A, TPA3123D (IC 7D10)

Block Diagram



Pin Configuration



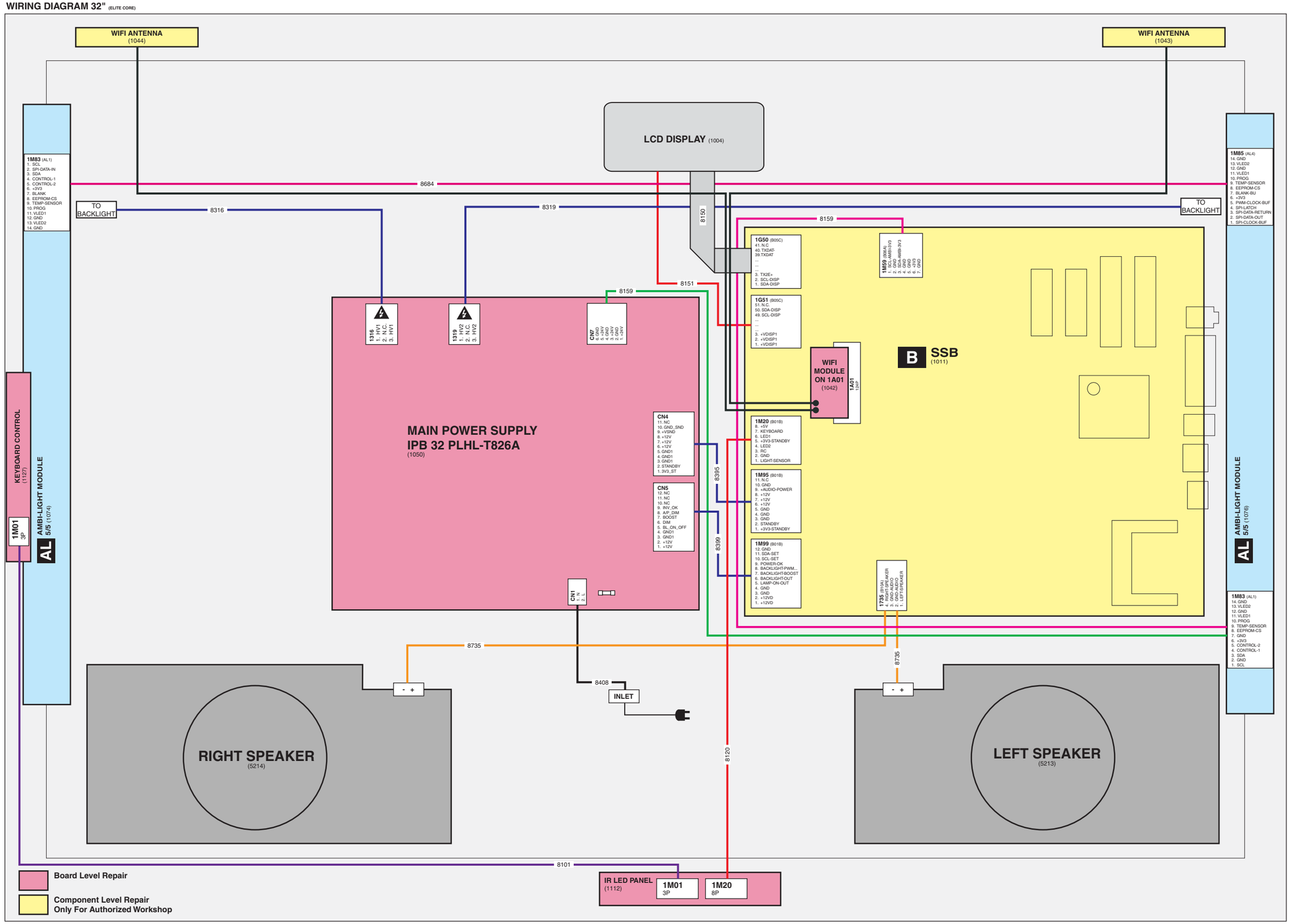
TERMINAL		I/O/P	DESCRIPTION
NAME	24-PIN (PWP)		
$\overline{SD}$	2	I	Shutdown signal for IC (low = disabled, high = operational). TTL logic levels with compliance to AVCC
RIN	6	I	Audio input for right channel
LIN	5	I	Audio input for left channel
GAIN0	18	I	Gain select least-significant bit. TTL logic levels with compliance to AVCC
GAIN1	17	I	Gain select most-significant bit. TTL logic levels with compliance to AVCC
MUTE	4	I	Mute signal for quick disable/enable of outputs (high = outputs switch at 50% duty cycle, low = outputs enabled). TTL logic levels with compliance to AVCC
BSL	21	I/O	Bootstrap I/O for left channel
PVCCL	1, 3	P	Power supply for left-channel H-bridge, not internally connected to PVCCR or AVCC
LOUT	22	O	Class-D 1/2-H-bridge positive output for left channel
PGNDL	23, 24	P	Power ground for left-channel H-bridge
VCLAMP	11	P	Internally generated voltage supply for bootstrap capacitors
BSR	16	I/O	Bootstrap I/O for right channel
ROUT	15	O	Class-D 1/2-H-bridge negative output for right channel
PGNDR	13, 14	P	Power ground for right-channel H-bridge.
PVCCR	10, 12	P	Power supply for right-channel H-bridge, not connected to PVCCL or AVCC
AGND	9	P	Analog ground for digital/analog cells in core
AGND	8	P	Analog ground for analog cells in core
BYPASS	7	O	Reference for preamplifier inputs. Nominally equal to AVCC/8. Also controls start-up time via external capacitor sizing.
AVCC	19, 20	P	High-voltage analog power supply. Not internally connected to PVCCR or PVCCL
Thermal pad	Die pad	P	Connect to ground. Thermal pad should be soldered down on all applications to properly secure device to printed wiring board.

18440_302_090303.eps
090303

Figure 8-6 Internal block diagram and pin configuration

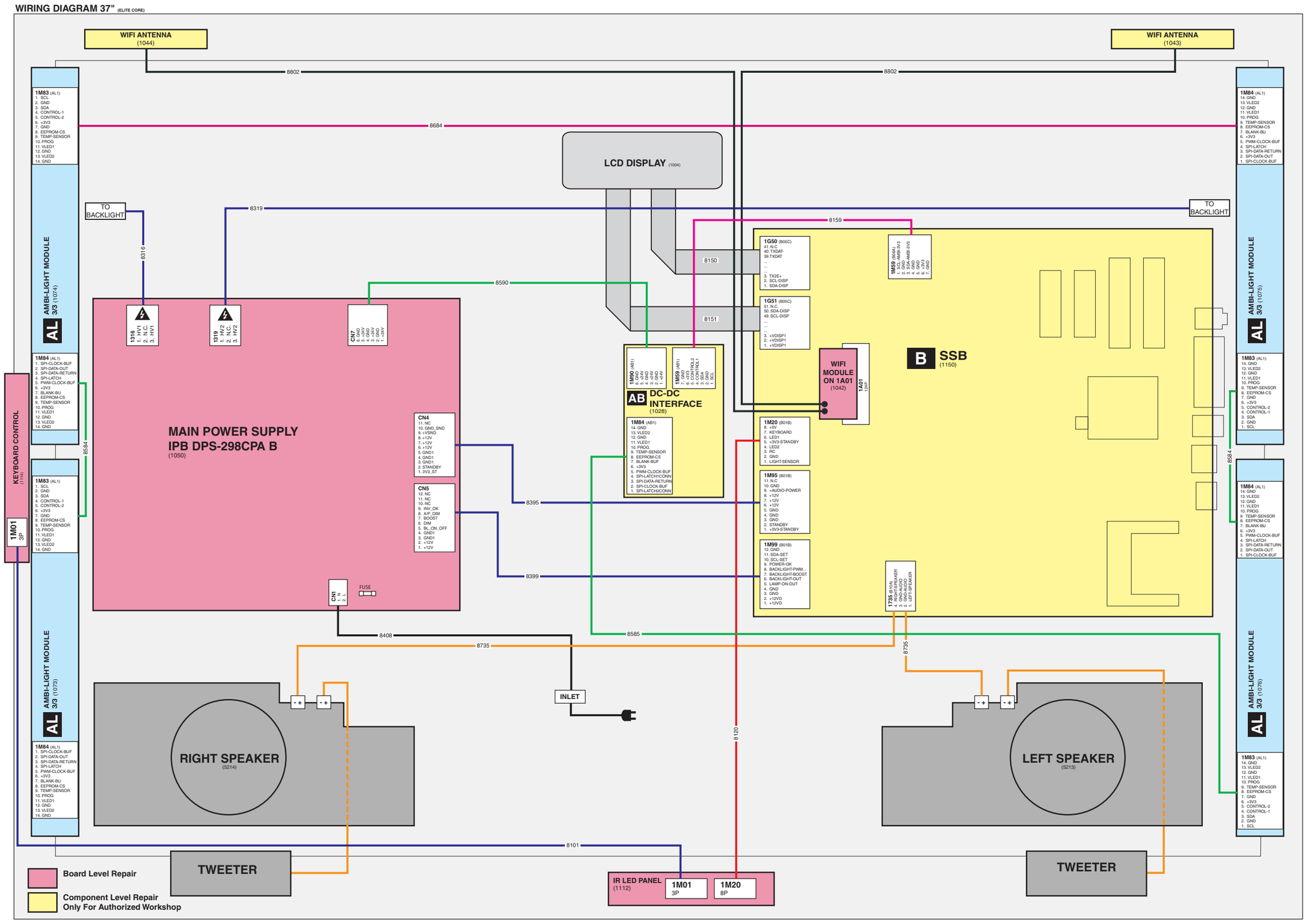
9. Block Diagrams

Wiring Diagram 32" (Elite Core)



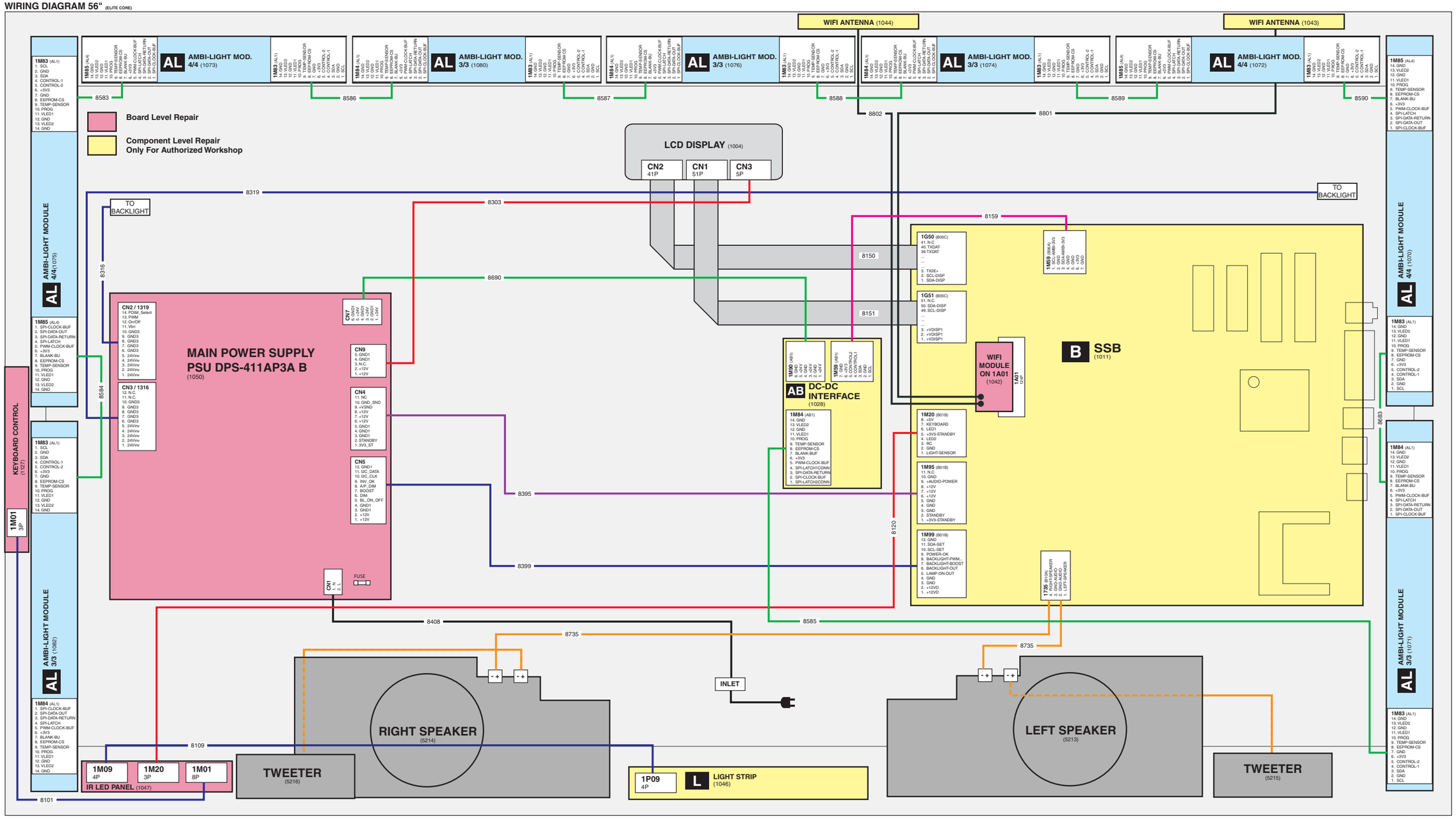
18310_400_090305.eps
090421

Wiring Diagram 37" (Elite Core)



Wiring Diagram 56" (Elite Core)

WIRING DIAGRAM 56" (ELITE CORE)



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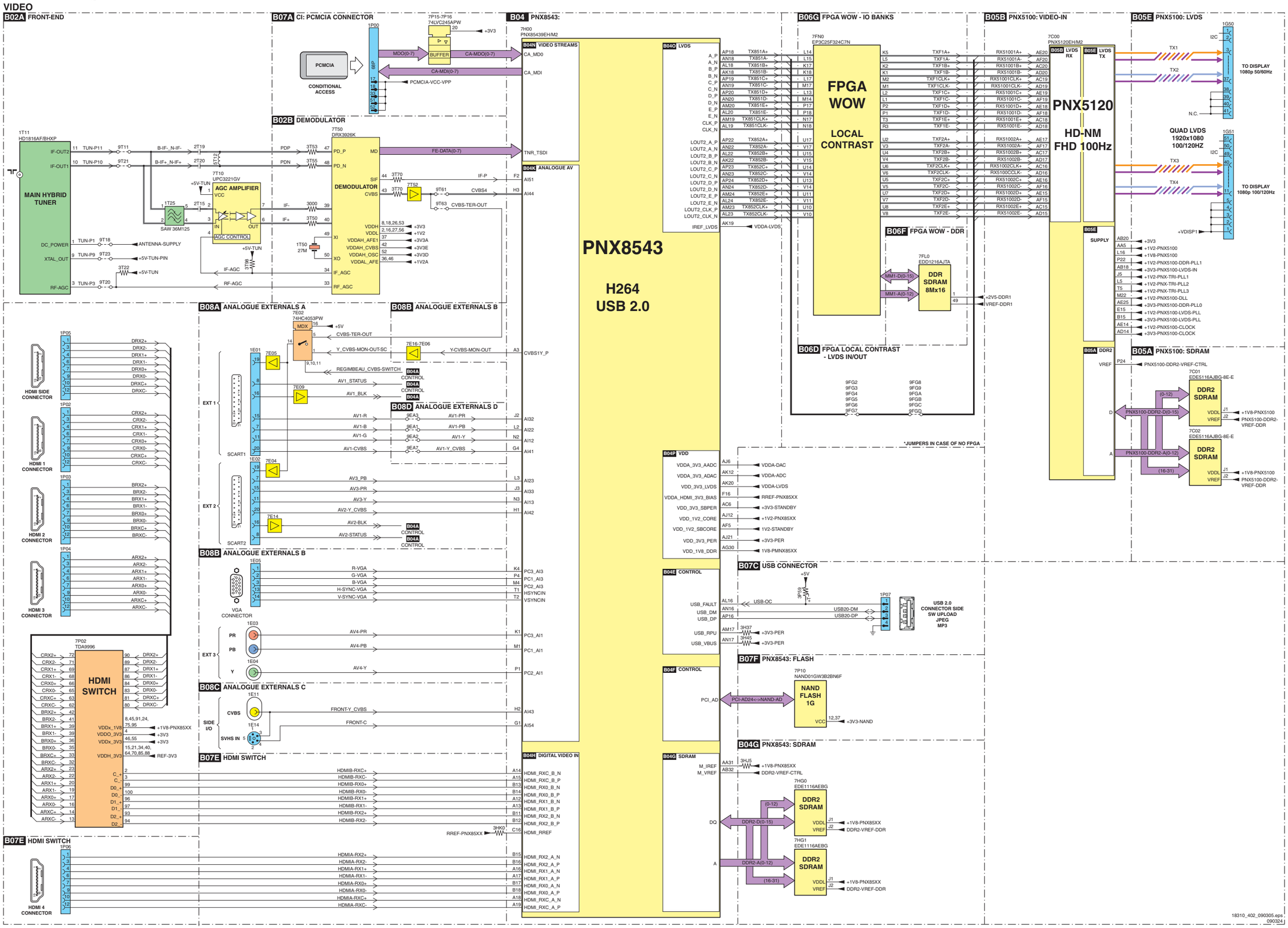
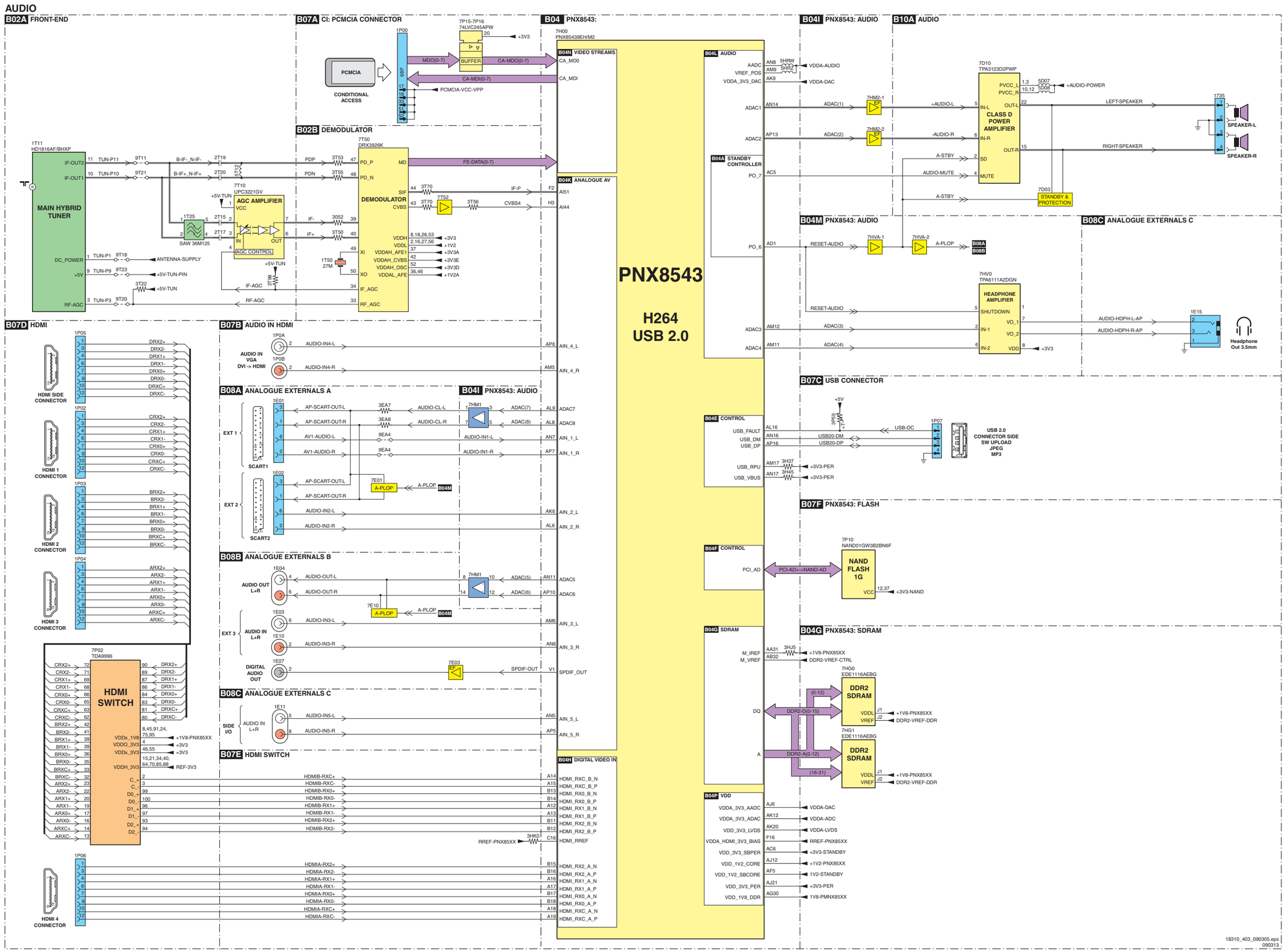
090508

Block Diagram Video

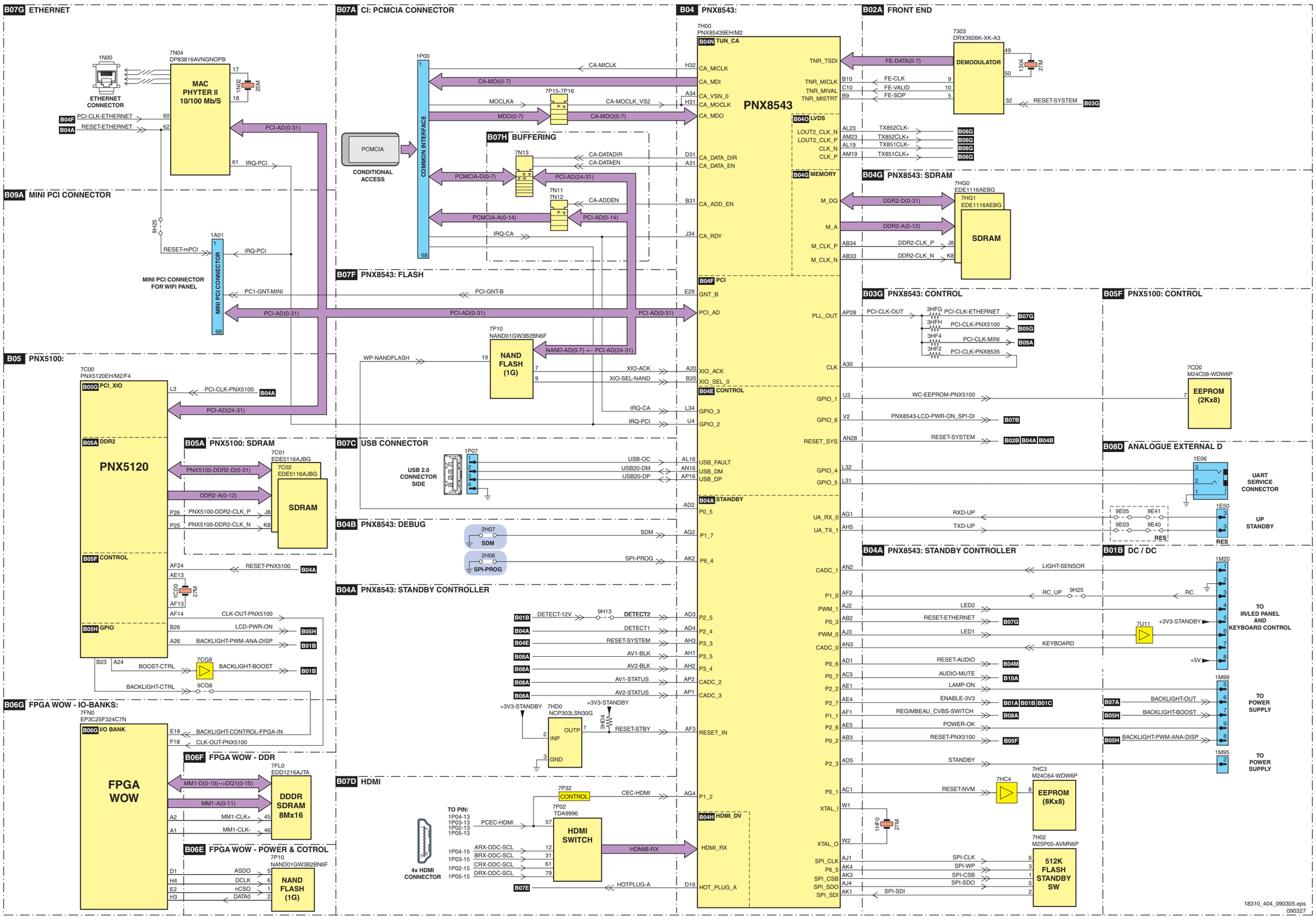


Block Diagram Audio



Block Diagram Control & Clock Signals

CONTROL + CLOCK SIGNALS



Block Diagram I²C

I²C

B04E PNX8543: CONTROL

7H00 PNX85439EH

SDA 3 G32 SDA3 3HPJ SDA-SSB

SCL 3 D33 SCL3 3HPH SCL-SSB

SSB BUS 400 kHz

ERR 13

PNX8543

B04G PNX8543: SDRAM

7HG0 EDE1116AEBG

7HG1 EDE1116AEBG SDRAM

MEMORY M_DQ DDR2-D M_A DDR2-A

B04H

DDC_SDA_B D15 DDC-SDA 6

DDC_SCL_B C15 DDC-SCL 5

HDMI_DV

DDC_SDA_A E19 DDCA-SDA

DDC_SCL_A C18 DDCA-SCL

B07F PNX5100: SDRAM

7P10 NAND01GW3B2BN

B04F

PCI PCI-AD FLASH 1G

B07D HDMI

+3V3-PER 3HPM 3HPK

7P02 TDA9996 HDMI MUX ERR 23

+5V-DDC 3P61 3P58 ARX-DDC-SDA 11 1P04 HDMI CONNECTOR 3

ARX-DDC-SCL 12

+5V-DDC 3P64 3P63 BRX-DDC-SDA 30 1P03 HDMI CONNECTOR 2

BRX-DDC-SCL 31

+5V-DDC 3P68 3P67 CRX-DDC-SDA 60 1P02 HDMI CONNECTOR 1

CRX-DDC-SCL 61

+5V-DDC 3P66 3P65 DRX-DDC-SDA 78 1P05 HDMI CONNECTOR SIDE

DRX-DDC-SCL 79

B07E HDMI SWITCH

+5V-DDC 3P29 3P28 ERX-DDC-SDA 1P06 HDMI CONNECTOR 4

ERX-DDC-SCL

7P07 M24C02 EEPROM 256x8

1M96 RES

B02B DEMODULATOR

7T50 DRX3926K DEMODULATOR MICRONAS ERR 27

+3V3 3T61 3T59 9T16 9T15 RES 9T71 TUN-SDA 9T70 TUN-SCL

TUNER BUS 400 kHz

B02A FRONT-END

1T11 HD1816AF MAIN TUNER ERR 34

TUN-P7 TUN-P6

B08B ANALOGUE EXTERNALS B

+5VDCOUT 1E05 3E70 3E47 DATA-SDA CLK-SCL

7E18 M24C02 EEPROM 256x8

VGA CONNECTOR

B05F PNX5100: CONTROL

7C00 PNX5120EH PNX5120 FHD 120Hz ERR 15 ERR 21

3CD8 3CD7 3CDD 3CDC

7CD0 M24C08 BOOT EEPROM ERR 25

B06E FPGA WOW POWER & CONTROL

B06F FPGA WOW - DDR

7FH0 M25P16 16M FLASH

7FL0 EDD1216AJTA DDR SDRAM 8Mx16

MM1-D MM1-A

B06G FPGA WOW - IO BANKS

7FN0 EP3C25F324C7N FPGA LOCAL CONTRAST ERR 29

D18 C18 9FNA 9FN9

B06A FPGA BACKLIGHT - LVDS & I2C - MUX

7F00 XC3S250E SPARTAN-3 FPGA

7F01 M25P20 2M FLASH

B08D ANALOGUE EXTERNALS D-

1HP0 3U67 3U66 SDA SCL

RESERVED

AMBILIGHT BUS 30 kHz

L1 3CDA SDA-AMBI-3V3

L2 3CD9 SCL-AMBI-3V3

+3V3 3RAA 3RAB 9F22 9F21 3FA6 3FA5 1M59 TO AMBI-LIGHT MODULE

B05A PNX5100: SDRAM

7C01 EDE5116AJBG

7C02 EDE5116AJBG SDRAM

PNX5100-DDR2-D(0-31)(0-31)

PNX5100-DDR2-A(0-12)

B04N PNX8543: VIDEO STREAMS

B07F PNX8543: FLASH

3HB2 3HB1 I2C-SDA I2C-SCL 1M97

B06D FPGA LOCAL CONTRAST LVDS IN/OUT

SET BUS 100 kHz

SDA 2 B33 SDA2 3HPU SDA-SET

SCL 2 D32 SCL2 3HPS SCL-SET

ERR 14

+3V3-PER 3HPV 3HPT

STANDBY BUS 400 kHz

SDA 1 H33 SDA1 3HPE SDA-UP-MIPS

SCL 1 F33 SCL1 3HPD SCL-UP-MIPS

+3V3-PER 3H50 3H49

B01B DC/DC

3U67 3U66 1M99 RES TO POWER SUPPLY

B06C TEMPERATURE & FAN CONTROL

3F61 3F62 3F67 3F66

7F50 LM75ADP IC TEMP SENSOR

7F51 PCA9533DP I2C LED DIMMER

RESERVED

B06A FPGA BACKLIGHT - LVDS & I2C - MUX

1F53 3F17 3F18 1M71 3F41 3F40 5F05 TO TEMP SENSOR

9FA2 9FA1

7F08 PCA9540BDP I2C MULTIPLEXER

SDA-SET0 SCL-SET0 SDA-SET1 SCL-SET1

9F20 9F19 9F18 9F17 9F15 9F13 9F16 9F14

SDA-BOLT-ON SCL-BOLT-ON SDA-DISP SCL-DISP

3F39 3F38 3F37 3F36

1R08 3E83 3E84 TO BOLT-ON MODULE

DISPLAY BUS 100 kHz

3FH4 3FH5 1F51 TO DISPLAY

RESERVED

B04A PNX8543: STANDBY CONTROLLER

B04A

MC_SDA AK5 3H66 SDA-UP-MIPS

MC_SCL AL5 3H55 SCL-UP-MIPS

STANDBY

+3V3-STANDBY 3H53 3H53 RES

+3V3-PER 3HC2-2 3HC4 7HC4 EF

PO_1 AC1 RESET-NVM 3HC2-1

3H53 3H52

7HC3 M24C64 EEPROM (NVM)

7H02 M25P05 512K FLASH

ERR 53

B08D ANALOGUE EXTERNAL D

7E19 74HC4066PW QUAD BILATERAL SWITCHES

B04A UART-SWITCH UART-SWITCHn 3E68 7E20

3ECK 3ECP

FOR MHP BOLT-ON 1R12 1R08

RXD-UP TXD-UP

7E17 ST3232C RS232 INTERFACE R1-IN T1-OUT R1-OUT T1-IN R2-IN T2-OUT R2-OUT T2-IN

9E41 9E40 9E05 9E03

1E50 UP 1E51 MIPS

LEVEL SHIFTER FOR DEBUG ONLY

RESERVED

B05E PNX5100: LVDS

3CA3 3CA2 3CA4 3CA5 1G50 1G51 TO DISPLAY

+3V3-STANDBY 3H58 3H57

UA_RX_0 AG1 RXD-UP

UA_TX_1 AH5 TXD-UP

+3V3-PER 3HFC 3HFT

GPIO_4 L32 RXD-MIPS

GPIO_5 L31 TXD-MIPS

B06B LED PANEL CONTROL

+3V3-PER 3HPR 3HPP

UA2_RX AL27 RXD-MIPS2

UA2_TX AK27 TXD-MIPS2

5FC7 5FC5 1R20 RES

9E35 9E36 RXD TXD 3E41 3E91 1E06 UART SERVICE CONNECTOR

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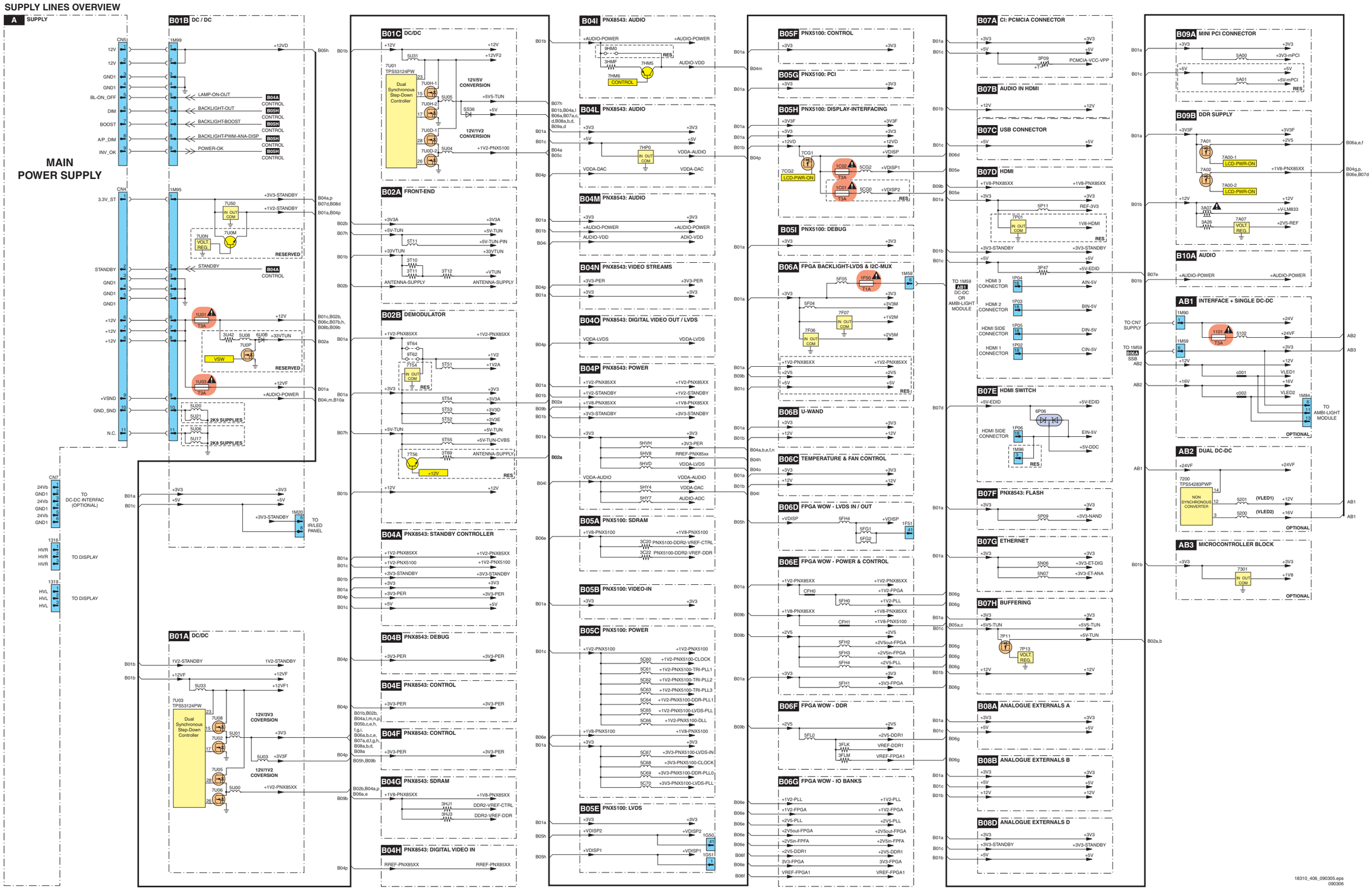
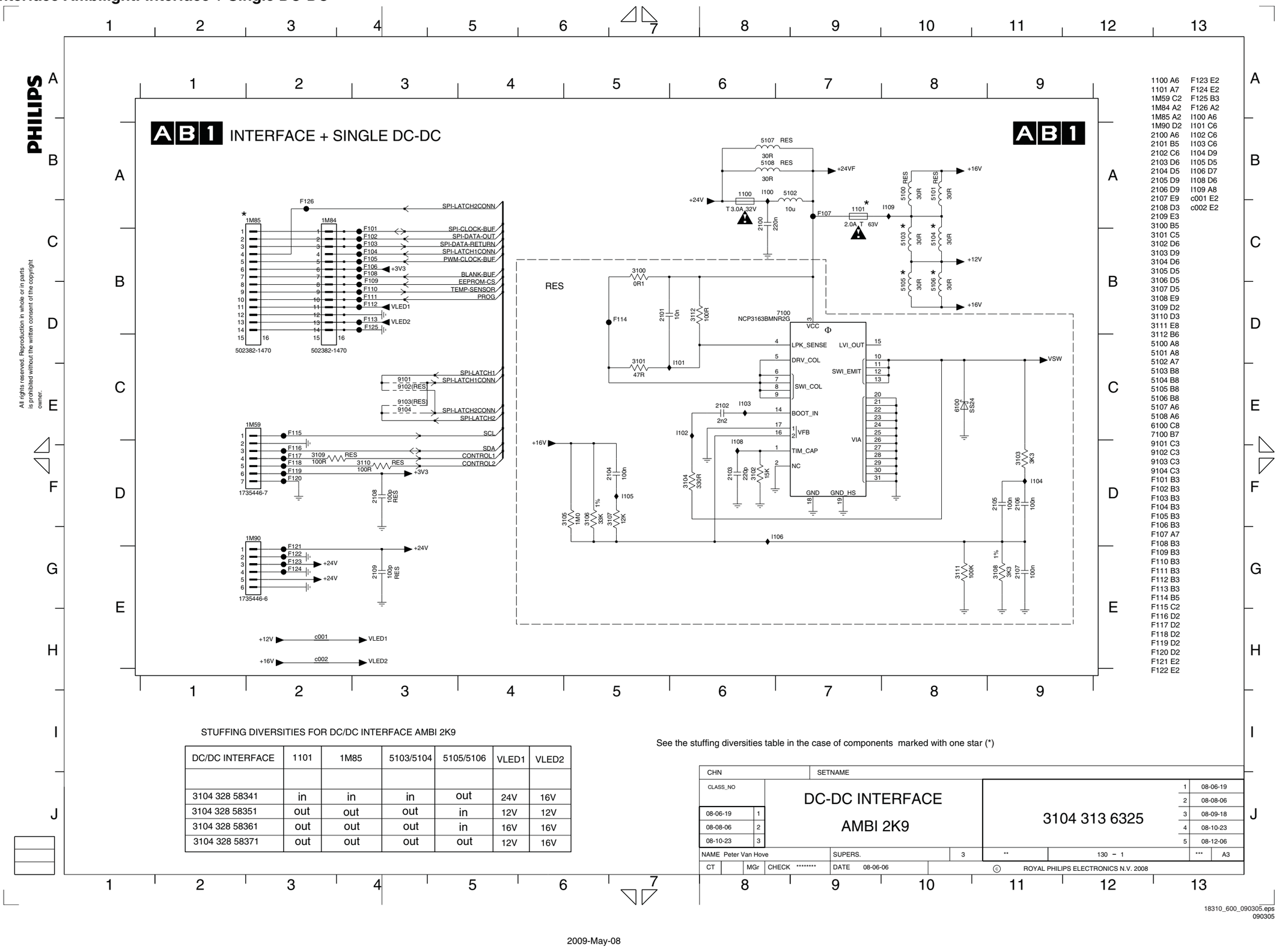
Supply Lines Overview



10. Circuit Diagrams and PWB Layouts

Interface Ambilight: Interface + Single DC-DC



STUFFING DIVERSITIES FOR DC/DC INTERFACE AMBI 2K9

DC/DC INTERFACE	1101	1M85	5103/5104	5105/5106	VLED1	VLED2
3104 328 58341	in	in	in	out	24V	16V
3104 328 58351	out	out	out	in	12V	12V
3104 328 58361	out	out	out	in	16V	16V
3104 328 58371	out	out	out	out	12V	16V

See the stuffing diversities table in the case of components marked with one star (*)

CHN	SETNAME		
CLASS_NO	DC-DC INTERFACE AMBI 2K9	3104 313 6325	1 08-06-19
08-06-19 1			2 08-08-06
08-08-06 2			3 08-09-18
08-10-23 3			4 08-10-23
			5 08-12-06
NAME Peter Van Hove	SUPERS. 3	** 130 – 1	*** A3
CT MGr CHECK ********	DATE 08-06-06	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

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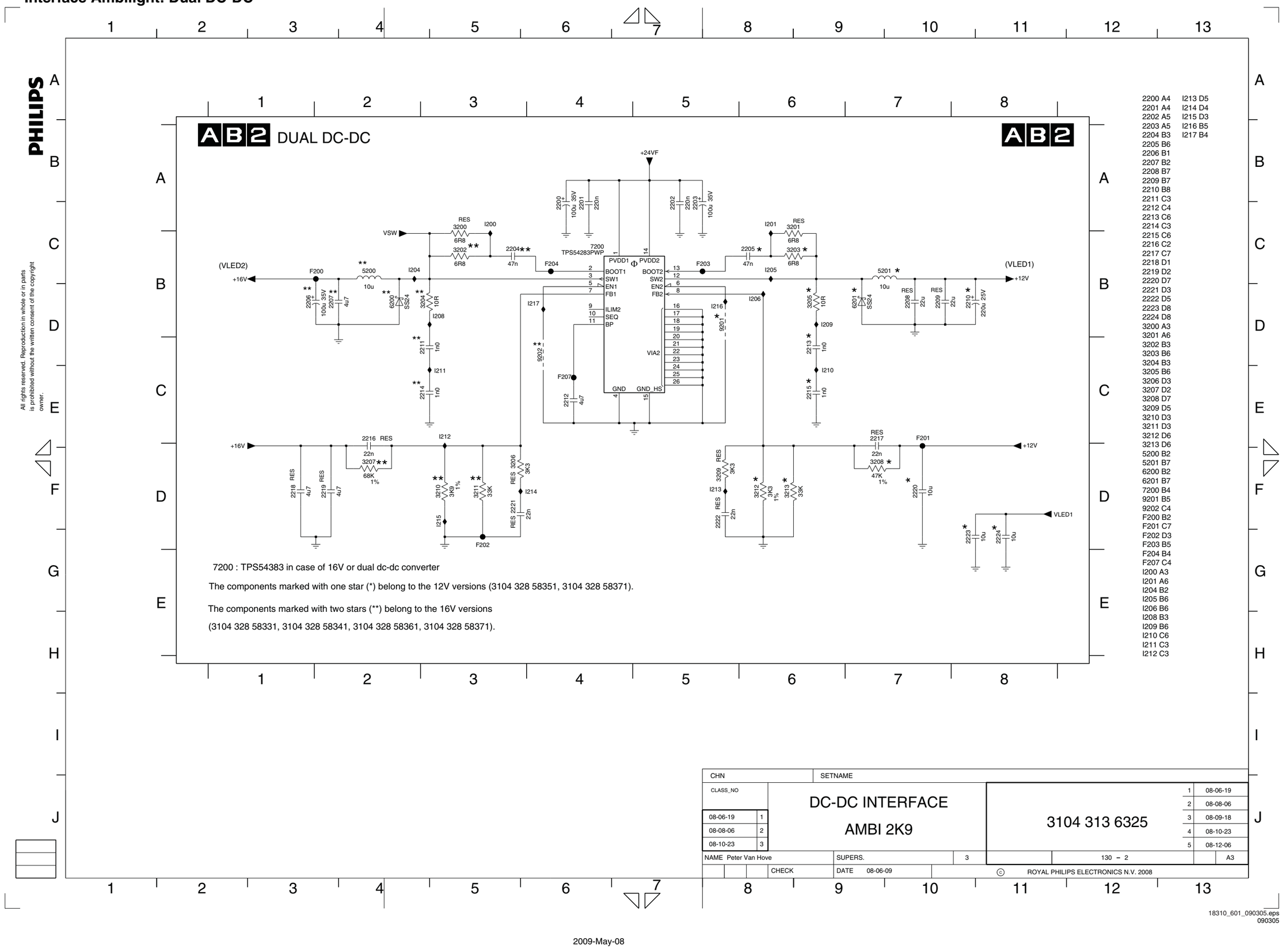
090305

Interface Ambilight: Dual DC-DC



7200 : TPS54383 in case of 16V or dual dc-dc converter

The components marked with one star (*) belong to the 12V versions (3104 328 58351, 3104 328 58371).

The components marked with two stars (**) belong to the 16V versions
(3104 328 58331, 3104 328 58341, 3104 328 58361, 3104 328 58371).

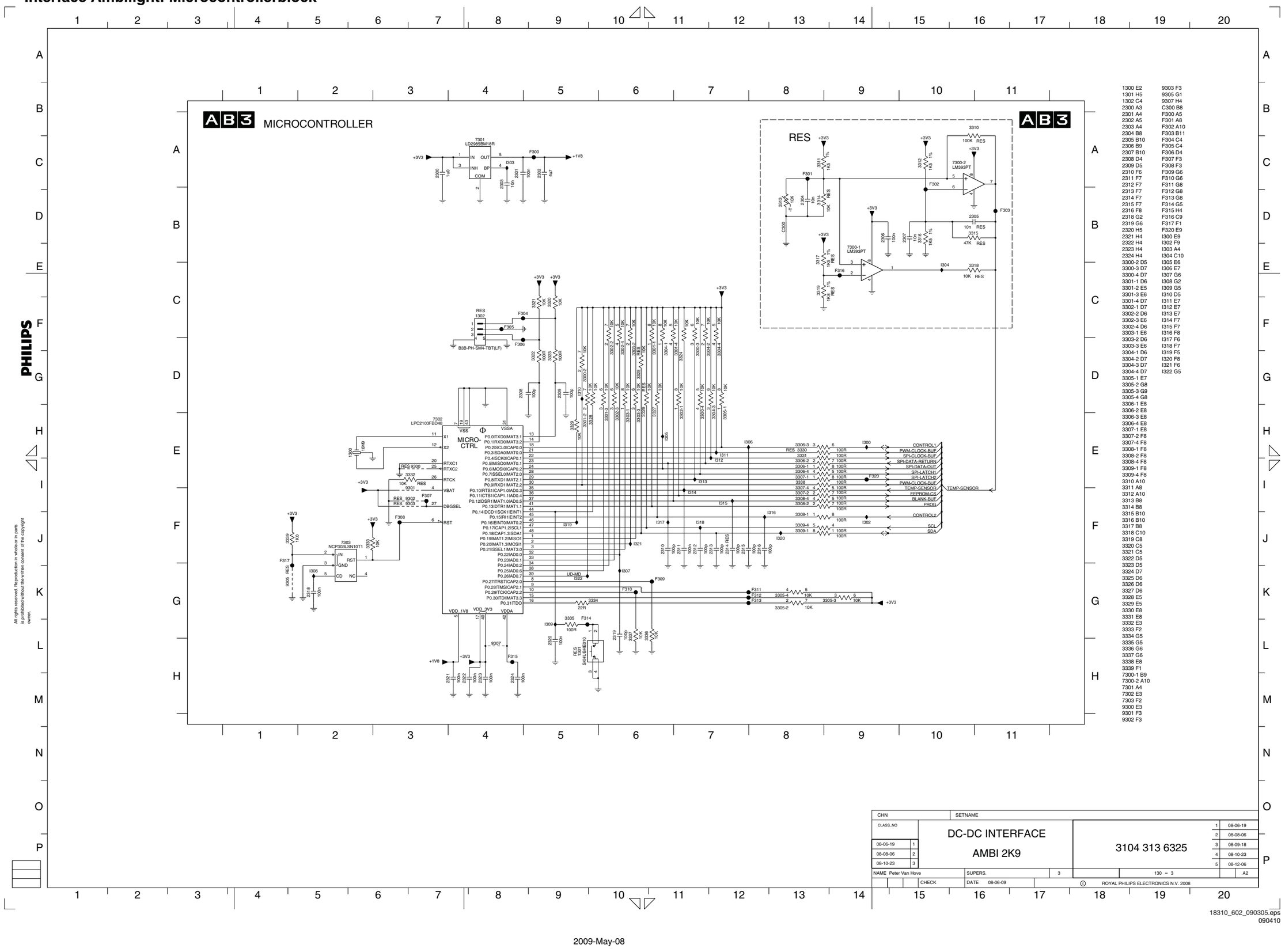
CHN		SETNAME	
CLASS_NO		DC-DC INTERFACE AMBI 2K9	3104 313 6325
08-06-19	1		
08-08-06	2		
08-10-23	3		
NAME Peter Van Hove		SUPERS.	3
		CHECK	DATE 08-06-09

1	08-06-19
2	08-08-06
3	08-09-18
4	08-10-23
5	08-12-06

130 – 2 A3

18310_601_090305.eps
090305

Interface Ambilight: Microcontrollerblock



1300 E2
1301 H5
1302 C4
2300 A3
2301 A4
2302 A5
2303 A4
2304 B8
2305 B10
2306 B9
2307 B10
2308 D4
2309 D5
2310 F6
2311 F7
2312 F7
2313 F7
2314 F7
2315 F7
2316 F8
2318 G2
2319 G6
2320 H5
2321 H4
2322 H4
2323 H4
2324 H4
3300-2 D5
3300-3 D7
3300-4 D7
3301-1 D6
3301-2 E5
3301-3 E6
3301-4 D7
3302-1 D7
3302-2 D6
3302-3 E6
3302-4 D6
3303-1 E6
3303-2 D6
3303-3 E6
3304-1 D6
3304-2 D7
3304-3 D7
3304-4 D7
3305-1 E7
3305-2 G8
3305-3 G9
3305-4 G8
3306-1 E8
3306-2 E8
3306-3 E8
3306-4 E8
3307-1 E8
3307-2 F8
3307-4 F8
3308-1 F8
3308-2 F8
3308-4 F8
3309-1 F8
3309-4 F8
3310 A10
3311 A8
3312 A10
3313 B8
3314 B8
3315 B10
3316 B10
3317 B8
3318 C10
3319 C8
3320 C5
3321 C5
3322 D5
3323 D5
3324 D7
3325 D6
3326 D6
3327 D6
3328 E5
3329 E5
3330 E8
3331 E8
3332 E3
3333 F2
3334 G5
3335 G5
3336 G6
3337 G6
3338 E8
3339 F1
7300-1 B9
7300-2 A10
7301 A4
7302 E3
7303 F2
9300 E3
9301 F3
9302 F3
9303 F3
9305 G1
9307 H4
C300 B8
F300 A5
F301 A8
F302 A10
F303 B11
F304 C4
F305 C4
F306 D4
F307 F3
F308 F3
F309 G6
F310 G6
F311 G8
F312 G8
F313 G8
F314 G5
F315 H4
F316 C9
F317 F1
F320 E9
I300 E9
I302 F9
I303 A4
I304 C10
I305 E6
I306 E7
I307 G6
I308 G2
I309 G5
I310 D5
I311 E7
I312 E7
I313 E7
I314 F7
I315 F7
I316 F8
I317 F6
I318 F7
I319 F5
I320 F8
I321 F6
I322 G5

CHN		SETNAME	
CLASS_NO		DC-DC INTERFACE AMBI 2K9	3104 313 6325
08-06-19	1		
08-08-06	2		
08-10-23	3		
NAME Peter Van Hove		SUPERS. 3	130 – 3
	CHECK	DATE 08-06-09	ROYAL PHILIPS ELECTRONICS N.V. 2008

1	08-06-19
2	08-08-06
3	08-09-18
4	08-10-23
5	08-12-06

A2

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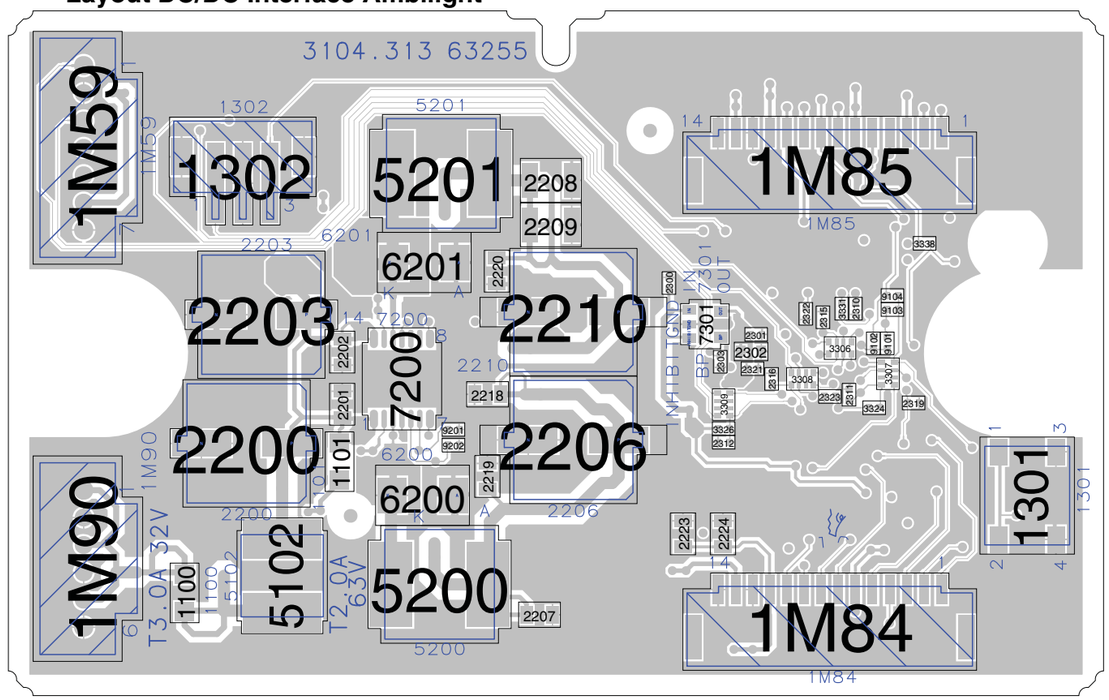
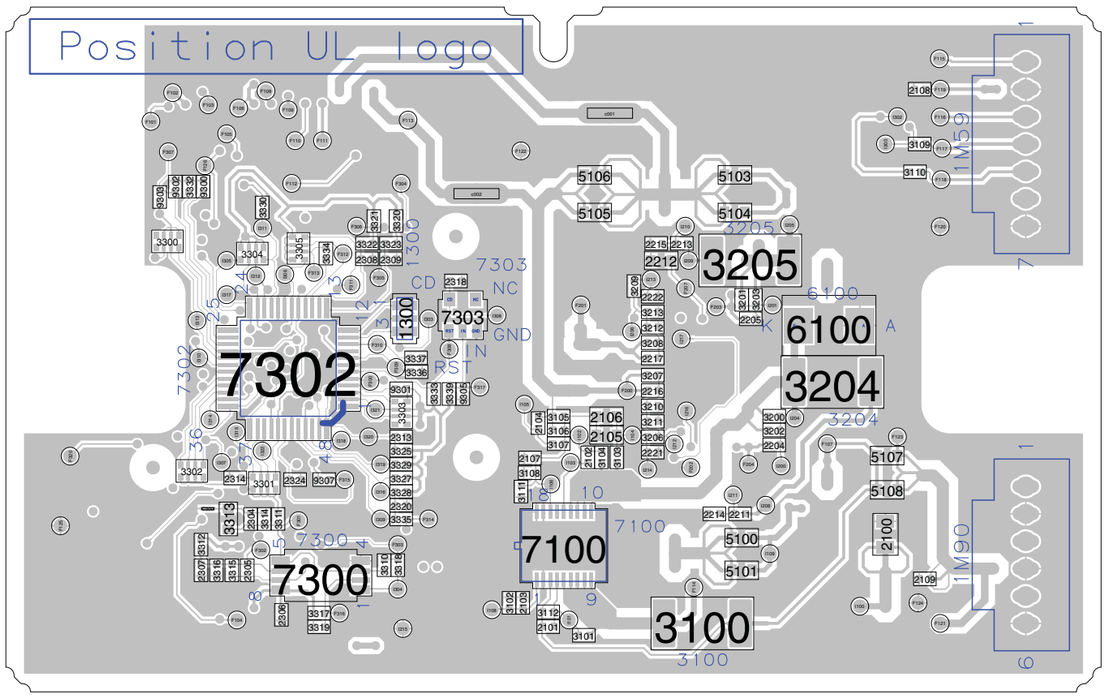
Layout DC/DC Interface Ambilight





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090309

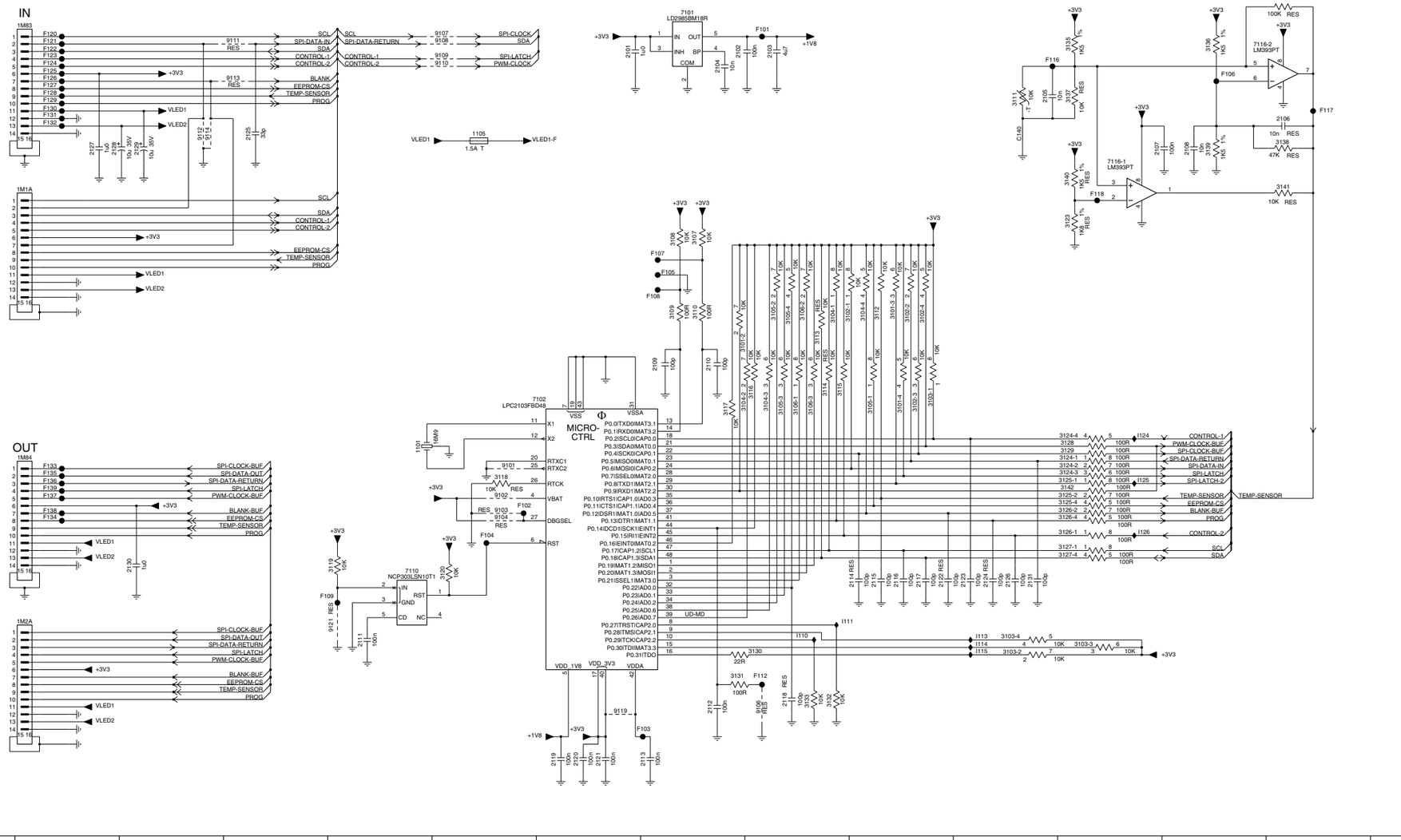
2009-May-08

Personal Notes:

10000_012_090121.eps
090121

6 LED Low-Pow: Microcontroller Block Liteon

AL 1 MICROCONTROLLER LITEON

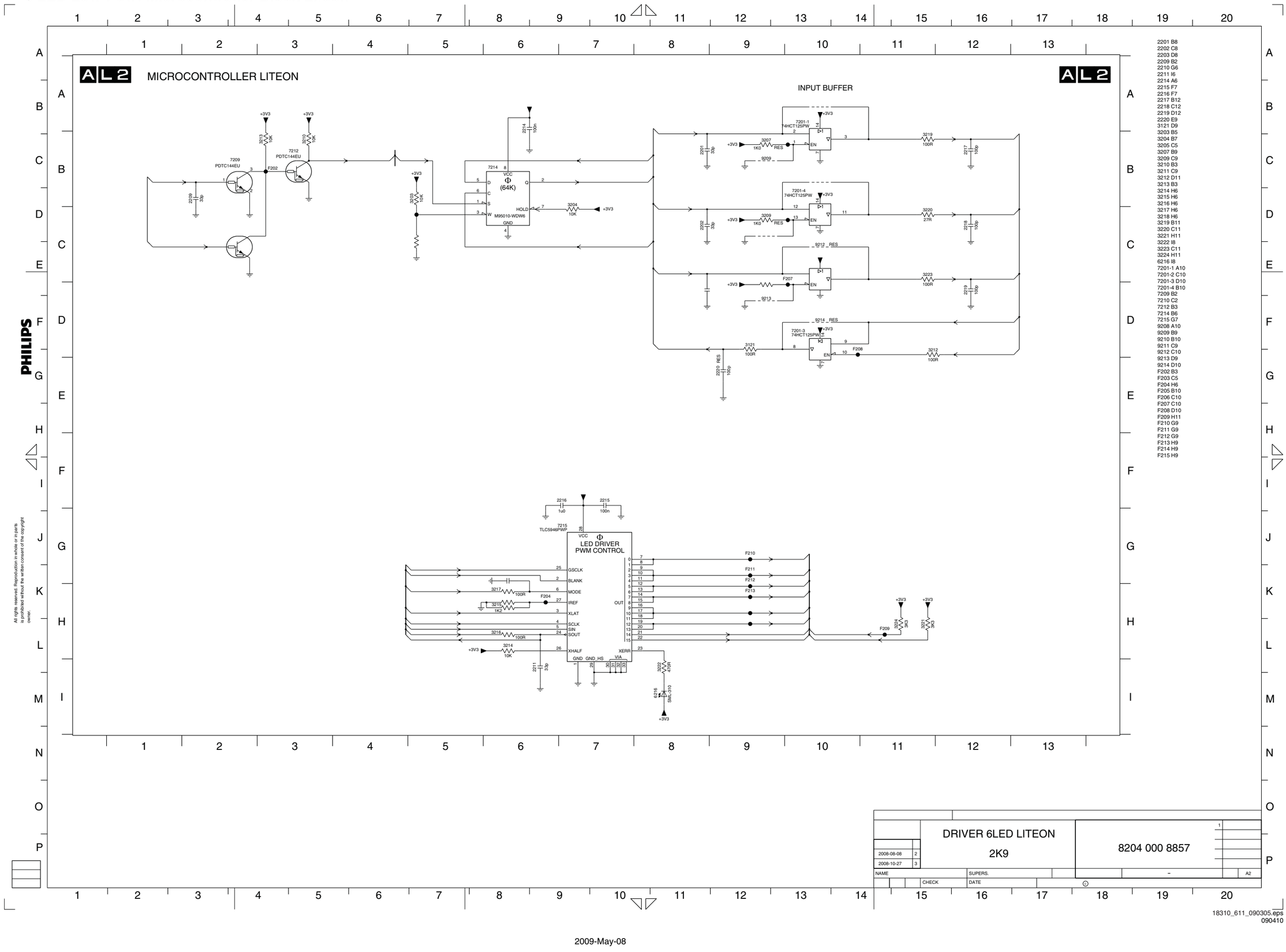


1101 E4	7116-2 A12	2131 F10	3101-2 D7
1105 B5	9101 E5	2125 B3	3101-3 D9
1M1A C1	9102 F5	2126 F10	3101-4 E9
1M2A G1	9103 F5	2127 B1	3102-1 D9
1M83 A1	9104 F5	2128 B1	3102-2 D9
1M84 E1	9106 H8	2129 B2	3102-3 E9
2101 A6	9107 A5	2130 F2	3102-4 D9
2102 A7	9108 A5		3103-1 E9
2103 A8	9109 A5		3103-2 G10
2104 B7	9110 B5		3103-3 G11
2105 B10	9111 A3		3103-4 G10
2106 B13	9112 B2		3104-1 D8
2107 B11	9113 B3		3104-2 E8
2108 B12	9114 B2		3104-3 E8
2109 D7	9119 H6		3104-4 D9
2110 D7	9121 G4		3105-1 E9
2111 G4	C140 B10		3105-2 D8
2112 H7	F101 A8		3105-3 E8
2113 H7	F102 F5		3105-4 D8
2114 F9	F103 H7		3106-1 E8
2115 F9	F104 F5		3106-2 D8
2116 F9	F105 D7		3106-3 E8
2117 F9	F106 B12		3107 C7
2118 H8	F107 C7		3108 C7
2119 H6	F108 D7		3109 D7
2120 H6	F109 G3		3110 D7
2121 H6	F112 G8		3111 B10
2122 F9	F116 A10		3112 D9
2123 F10	F117 B13		3113 D8
2124 F10	F118 C11		3114 E8
2125 B3	F120 A1		3115 E8
2126 F10	F121 A1		3116 E8
2127 B1	F122 A1		3117 E7
2128 B1	F123 A1		3118 E5
2129 B2	F124 B1		3119 F4
2130 F2	F125 B1		3120 F5
2131 F10	F126 B1		3123 C11
3101-2 D7	F127 B1		3124-1 E11
3101-3 D9	F128 B1		3124-2 E11
3101-4 E9	F129 B1		3124-3 E11
3102-1 D9	F130 B1		3124-4 E11
3102-2 D9	F131 B1		3125-1 F11
3102-3 E9	F132 B1		3125-2 F11
3102-4 D9	F133 E1		3125-4 F11
3103-1 E9	F134 F1		3126-1 F11
3103-2 G10	F135 E1		3126-2 F11
3103-3 G11	F136 F1		3126-4 F11
3103-4 G10	F137 F1		3127-1 F11
3104-1 D8	F138 F1		3127-4 F11
3104-2 E8	F139 F1		3128 E11
3104-3 E8	I110 G8		3129 E11
3104-4 D9	I111 G8		3130 G8
3105-1 E9	I113 G10		3131 G7
3105-2 D8	I114 G10		3132 H8
3105-3 E8	I115 G10		3133 H8
3105-4 D8	I124 E11		3134 A13
3106-1 E8	I125 E11		3135 A11
3106-2 D8	I126 F11		3136 A12
3106-3 E8			3137 B11
3107 C7			3138 B13
3108 C7			3139 B12
3109 D7			3140 C11
3110 D7			3141 C13
3111 B10			3142 F11
3112 D9			7101 A7
3113 D8			7102 E6
3114 E8			7110 F4
3115 E8			7116-1 B11
3116 E8			
3117 E7			
3118 E5			
3119 F4			
3120 F5			
3123 C11			
3124-1 E11			
3124-2 E11			
3124-3 E11			
3124-4 E11			
3125-1 F11			
3125-2 F11			
3125-4 F11			
3126-1 F11			
3126-2 F11			
3126-4 F11			
3127-1 F11			
3127-4 F11			
3128 E11			
3129 E11			
3130 G8			
3131 G7			
3132 H8			
3133 H8			
3134 A13			
3135 A11			
3136 A12			
3137 B11			
3138 B13			
3139 B12			
3140 C11			
3141 C13			
3142 F11			
7101 A7			
7102 E6			
7110 F4			
7116-1 B11			

CHN	SETNAME		
CLASS_NO	DRIVER 6LED LITEON 2K9	8204 000 8857	1 2008-06-10
2008-08-08 2			2 2008-08-08
2008-10-27 3			3 2008-10-27
NAME Peter Van Hove	SUPERS. 3	130 ~ 1	A2
CHECK	DATE 2008-06-02	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

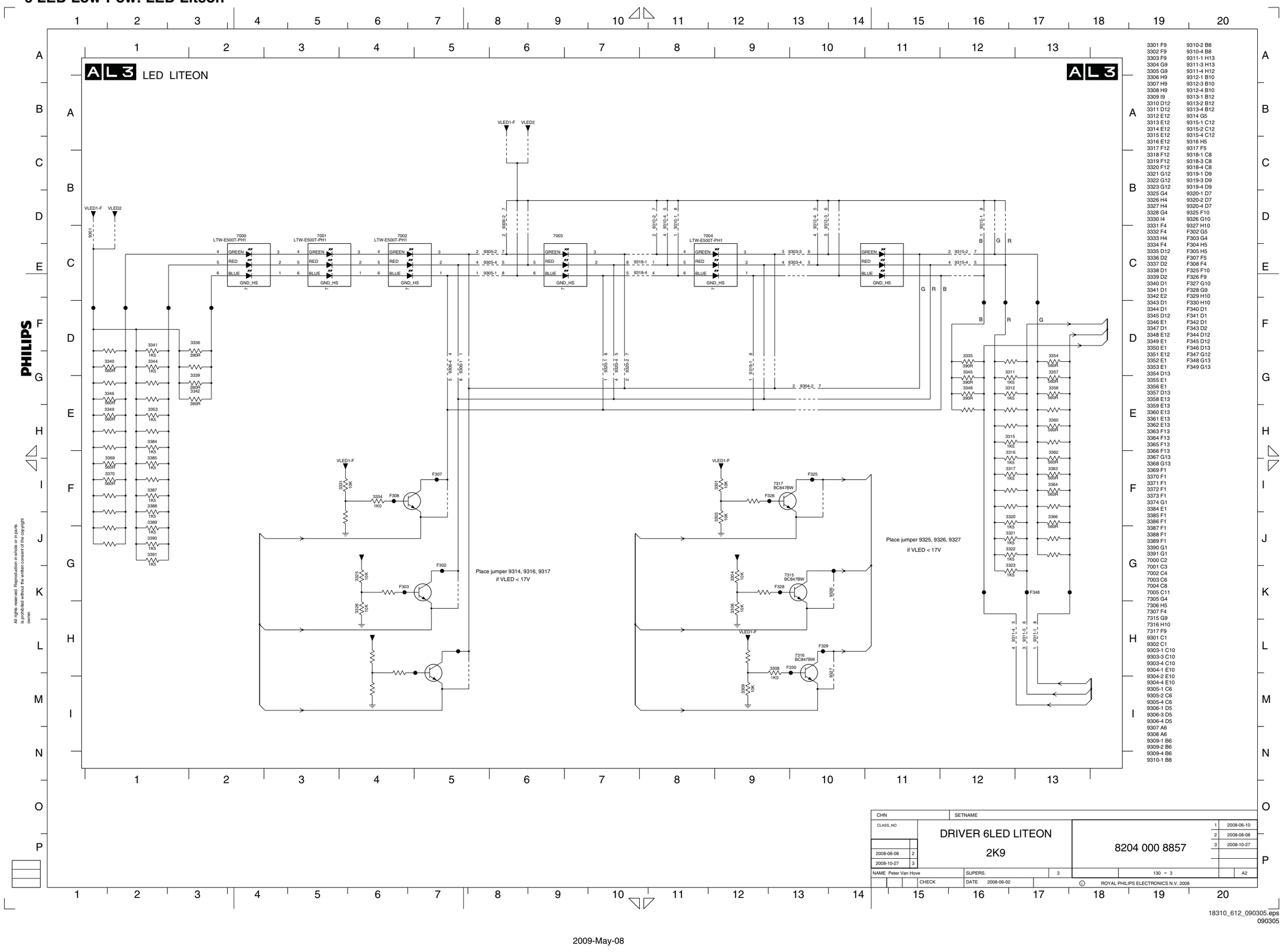
18310_610_090305.eps
090410

6 LED Low-Pow: Microcontroller Block Liteon



18310_611_090305.eps
090410

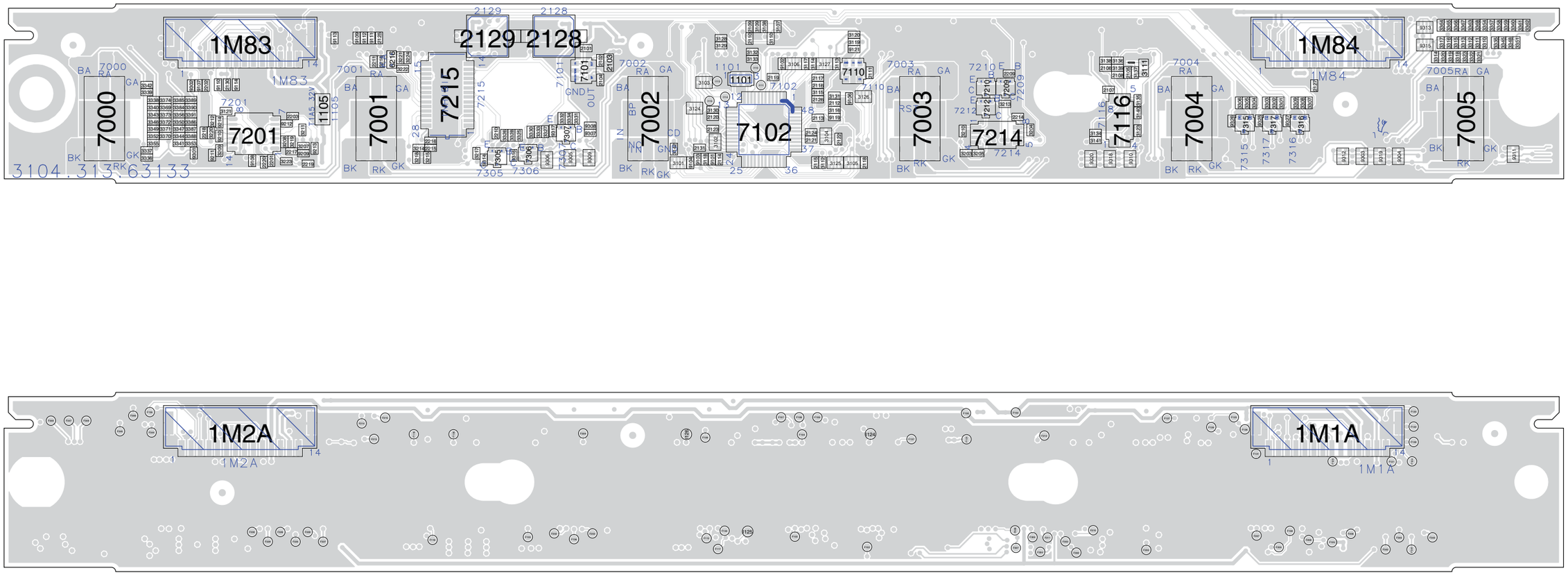
6 LED Low-Pow: LED Liteon



CHN	SETNAME		
CLASS_NO	DRIVER 6LED LITEON 2K9	8204 000 8857	1 2008-06-10
2008-08-08 2			2 2008-08-08
2008-10-27 3			3 2008-10-27
NAME Peter Van Hove	SUPERS. 3	130 ~ 3	A2
CHECK	DATE 2008-06-02	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_612_090305.eps
090305

Layout 6 LED Low-Pow

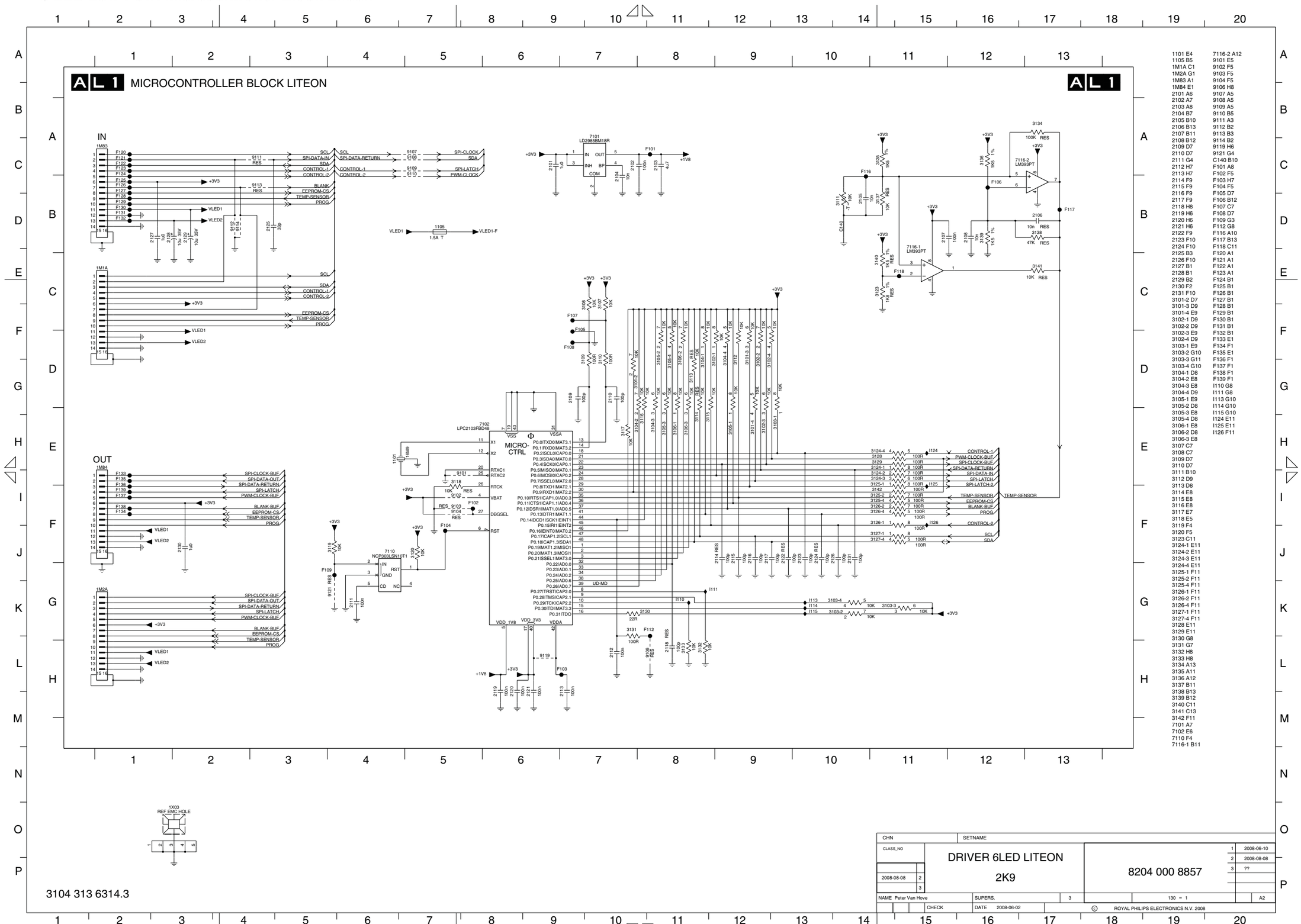


3104 313 6313.3

18310_551_090309
090309

8 LED Low-Pow: Microcontroller Block Liteon

AL 1 MICROCONTROLLER BLOCK LITEON



1101 E4
1105 B5
1M1A C1
1M2A G1
1M83 A1
1M84 E1
2101 A6
2102 A7
2103 A8
2104 B7
2105 B10
2106 B13
2107 B11
2108 B12
2109 D7
2110 D7
2111 G4
2112 H7
2113 H7
2114 F9
2115 F9
2116 F9
2117 F9
2118 H8
2119 H6
2120 H6
2121 H6
2122 F9
2123 F10
2124 F10
2125 B3
2126 F10
2127 B1
2128 B1
2129 B2
2130 F2
2131 F10
3101-2 D7
3101-3 D9
3101-4 E9
3102-1 D9
3102-2 D9
3102-3 E9
3102-4 D9
3103-1 E9
3103-2 G10
3103-3 G11
3103-4 G10
3104-1 D8
3104-2 E8
3104-3 E8
3104-4 D9
3105-1 E9
3105-2 D8
3105-3 E8
3105-4 D8
3106-1 E8
3106-2 D8
3106-3 E8
3107 C7
3108 C7
3109 D7
3110 D7
3111 B10
3112 D9
3113 D8
3114 E8
3115 E8
3116 E8
3117 E7
3118 E5
3119 F4
3120 F5
3123 C11
3124-1 E11
3124-2 E11
3124-3 E11
3124-4 E11
3125-1 F11
3125-2 F11
3125-4 F11
3126-1 F11
3126-2 F11
3126-4 F11
3127-1 F11
3127-4 F11
3128 E11
3129 E11
3130 G8
3131 G7
3132 H8
3133 H8
3134 A13
3135 A11
3136 A12
3137 B11
3138 B13
3139 B12
3140 C11
3141 C13
3142 F11
7101 A7
7102 E6
7110 F4
7116-1 B11
7116-2 A12
9101 E5
9102 F5
9103 F5
9104 F5
9106 H8
9107 A5
9108 A5
9109 A5
9110 B5
9111 A3
9112 B2
9113 B3
9114 B2
9119 H6
9121 G4
C140 B10
F101 A8
F102 F5
F103 H7
F104 F5
F105 D7
F106 B12
F107 C7
F108 D7
F109 G3
F112 G8
F116 A10
F117 B13
F118 C11
F120 A1
F121 A1
F122 A1
F123 A1
F124 B1
F125 B1
F126 B1
F127 B1
F128 B1
F129 B1
F130 B1
F131 B1
F132 B1
F133 E1
F134 F1
F135 E1
F136 F1
F137 F1
F138 F1
F139 F1
I110 G8
I111 G8
I113 G10
I114 G10
I115 G10
I124 E11
I125 E11
I126 F11

3104 313 6314.3

CHN	SETNAME		
CLASS_NO	DRIVER 6LED LITEON 2K9	8204 000 8857	1 2008-06-10; 2 2008-08-08; 3 ??
2008-08-08 2 3			
NAME Peter Van Hove	SUPERS. 3	130 – 1	A2
CHECK	DATE 2008-06-02	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

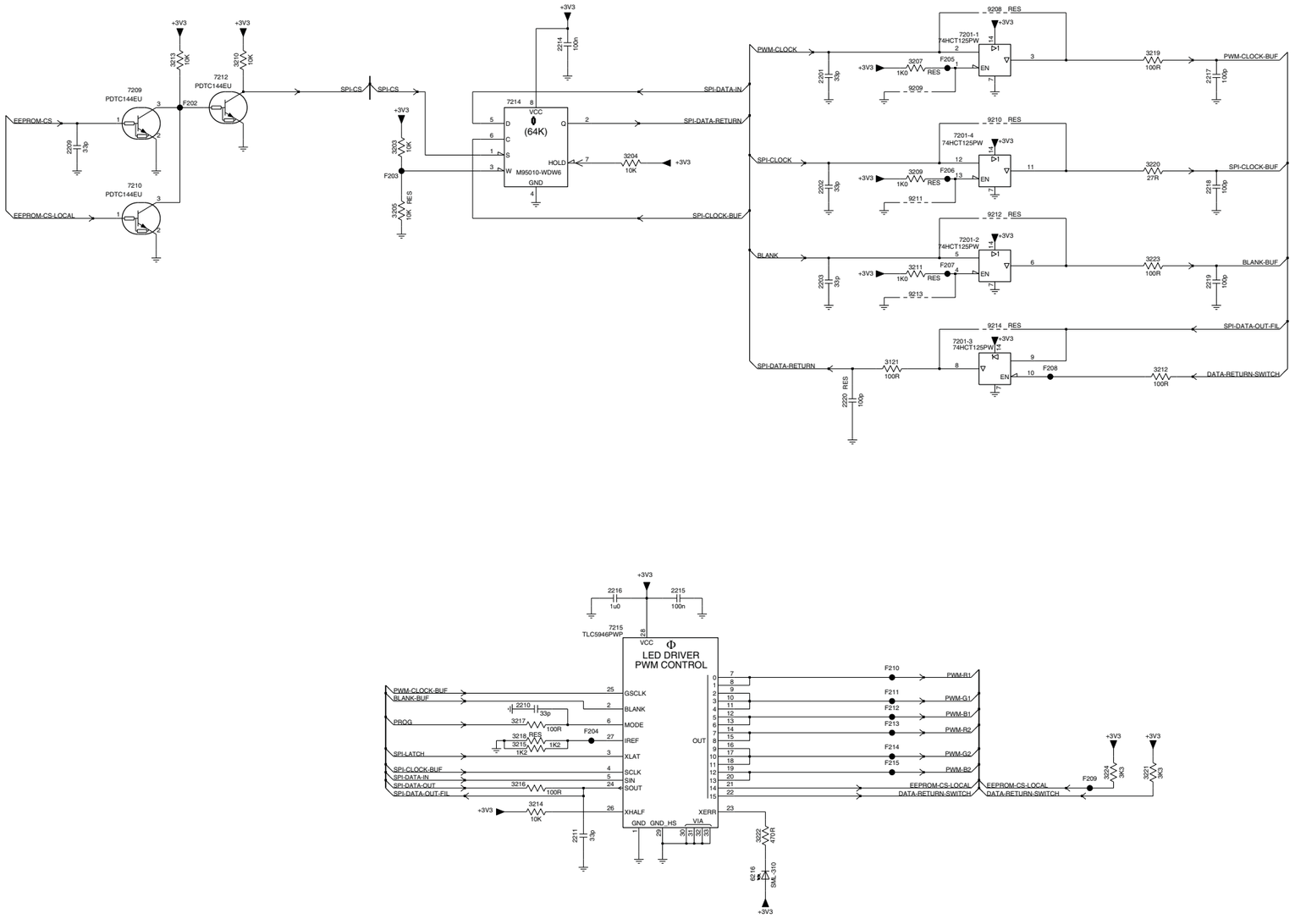
18310_650_090508.eps
090507

8 LED Low-Pow: Microcontroller Block Liteon

AL2 MICROCONTROLLER BLOCK LITEON

AL2

INPUT BUFFER



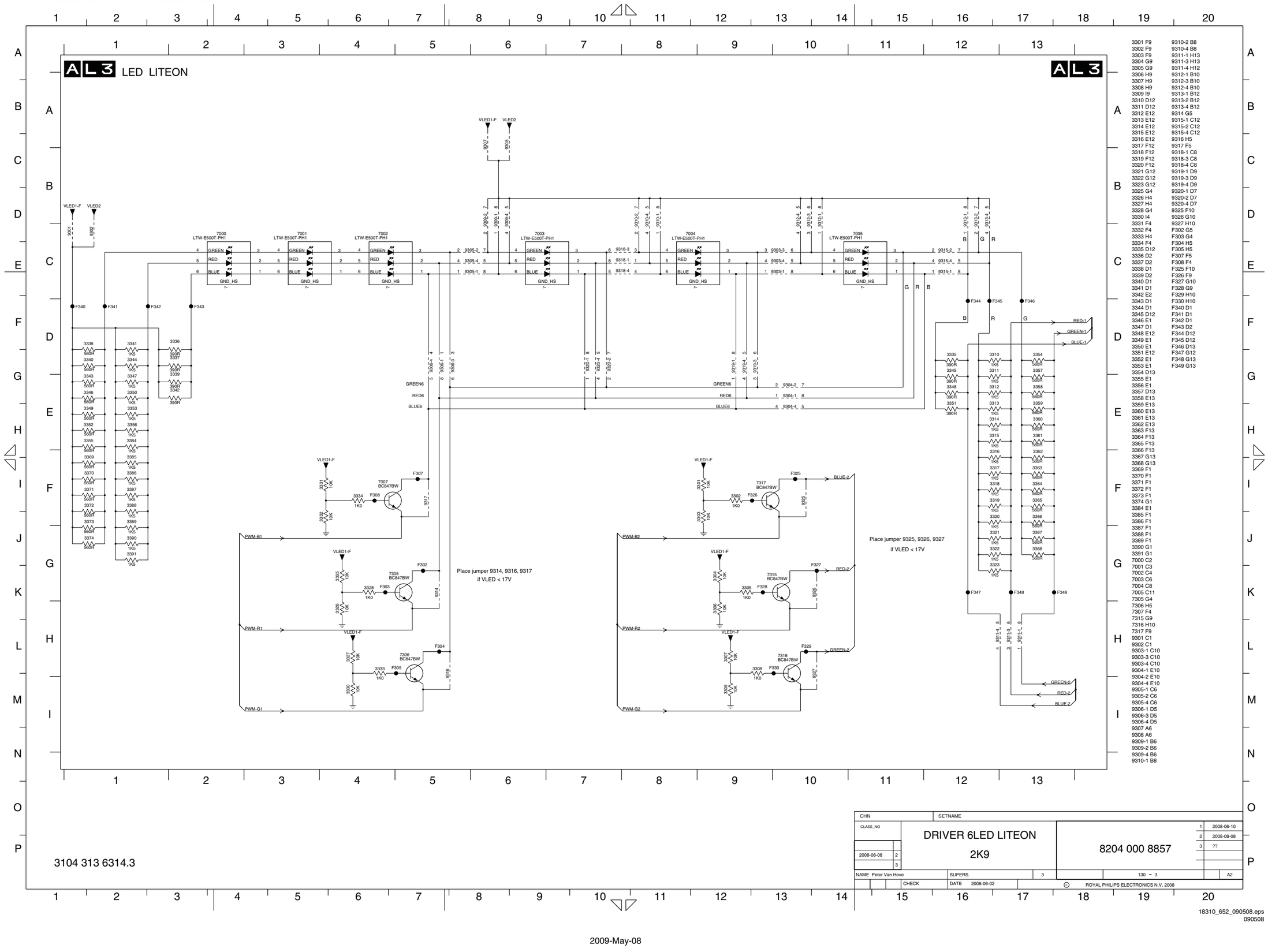
2201 B8
2202 C8
2203 D8
2209 B2
2210 G6
2211 I6
2214 A6
2215 F7
2216 F7
2217 B12
2218 C12
2219 D12
2220 E9
3121 D9
3203 B5
3204 B7
3205 C5
3207 B9
3209 C9
3210 B3
3211 C9
3212 D11
3213 B3
3214 H6
3215 H6
3216 H6
3217 H6
3218 H6
3219 B11
3220 C11
3221 H11
3222 I8
3223 C11
3224 H11
6216 I8
7201-1 A10
7201-2 C10
7201-3 D10
7201-4 B10
7209 B2
7210 C2
7212 B3
7214 B6
7215 G7
9208 A10
9209 B9
9210 B10
9211 C9
9212 C10
9213 D9
9214 D10
F202 B3
F203 C5
F204 H6
F205 B10
F206 C10
F207 C10
F208 D10
F209 H11
F210 G9
F211 G9
F212 G9
F213 H9
F214 H9
F215 H9

CHN	SETNAME		
CLASS_NO	DRIVER 6LED LITEON 2K9	8204 000 8857	1 2008-06-10 2 2008-08-08 3 ??
2008-08-08 2 3			
NAME Peter Van Hove	SUPERS. 3	130 - 2	A2
CHECK	DATE 2008-06-02	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

3104 313 6314.3

18310_651_090508.eps
090508

8 LED Low-Pow: LED Liteon



3301 F9
3302 F9
3303 F9
3304 G9
3305 G9
3306 H9
3307 H9
3308 H9
3309 I9
3310 D12
3311 D12
3312 E12
3313 E12
3314 E12
3315 E12
3316 E12
3317 F12
3318 F12
3319 F12
3320 F12
3321 G12
3322 G12
3323 G12
3325 G4
3326 H4
3327 H4
3328 G4
3330 I4
3331 F4
3332 F4
3333 H4
3334 F4
3335 D12
3336 D2
3337 D2
3338 D1
3339 D2
3340 D1
3341 D1
3342 E2
3343 D1
3344 D1
3345 D12
3346 E1
3347 D1
3348 E12
3349 E1
3350 E1
3351 E12
3352 E1
3353 E1
3354 D13
3355 E1
3356 E1
3357 D13
3358 E13
3359 E13
3360 E13
3361 E13
3362 E13
3363 F13
3364 F13
3365 F13
3366 F13
3367 G13
3368 G13
3369 F1
3370 F1
3371 F1
3372 F1
3373 F1
3374 G1
3384 E1
3385 F1
3386 F1
3387 F1
3388 F1
3389 F1
3390 G1
3391 G1
7000 C2
7001 C3
7002 C4
7003 C6
7004 C8
7005 C11
7305 G4
7306 H5
7307 F4
7315 G9
7316 H10
7317 F9
9301 C1
9302 C1
9303-1 C10
9303-3 C10
9303-4 C10
9304-1 E10
9304-2 E10
9304-4 E10
9305-1 C6
9305-2 C6
9305-4 C6
9306-1 D5
9306-3 D5
9306-4 D5
9307 A6
9308 A6
9309-1 B6
9309-2 B6
9309-4 B6
9310-1 B8
9310-2 B8
9310-4 B8
9311-1 H13
9311-3 H13
9311-4 H12
9312-1 B10
9312-3 B10
9312-4 B10
9313-1 B12
9313-2 B12
9313-4 B12
9314 G5
9315-1 C12
9315-2 C12
9315-4 C12
9316 H5
9317 F5
9318-1 C8
9318-3 C8
9318-4 C8
9319-1 D9
9319-3 D9
9319-4 D9
9320-1 D7
9320-2 D7
9320-4 D7
9325 F10
9326 G10
9327 H10
F302 G5
F303 G4
F304 H5
F305 H5
F307 F5
F308 F4
F325 F10
F326 F9
F327 G10
F328 G9
F329 H10
F330 H10
F340 D1
F341 D1
F342 D1
F343 D2
F344 D12
F345 D12
F346 D13
F347 G12
F348 G13
F349 G13

8 LED Low-Pow: LED Drive Liteon

AL 4 LED DRIVE

AL 4

1M3A E2
1M85 D2
3536 E9
3537 E9
3538 E7
3539 E9
3540 E7
3541 E8
3542 E9
3543 E7
3544 E8
3546 E7
3547 E8
3549 F7
3550 E8
3552 F7
3553 F8
3555 F7
3556 F8
3569 F7
3570 F7
3571 G7
3572 G7
3573 G7
3574 G7
3584 F8
3585 F8
3586 F8
3587 G8
3588 G8
3589 G8
3590 G8
3591 G8
7006 A5
7007 A7

7006 LTW-E500T-PH1

7007 LTW-E500T-PH1

GREEN-1
RED-1
BLUE-1
GND_HS

1M85

SPI-CLOCK-BUF
SPI-DATA-OUT
SPI-DATA-RETURN
SPI-LATCH
PWM-CLOCK-BUF
+3V3
BLANK-BUF
EEPROM-CS
TEMP-SENSOR
PROG
VLED1
VLED2

1M3A

GREEN-2
RED-2
BLUE-2

3538 560R
3540 560R
3543 560R
3546 560R
3549 560R
3552 560R
3555 560R
3569 560R
3570 560R
3571 560R
3572 560R
3573 560R
3574 560R

3541 1K5
3544 1K5
3547 1K5
3550 1K5
3553 1K5
3556 1K5
3584 1K5
3585 1K5
3586 1K5
3587 1K5
3588 1K5
3589 1K5
3590 1K5
3591 1K5

3536 390R
3537 390R
3539 390R
3542 390R

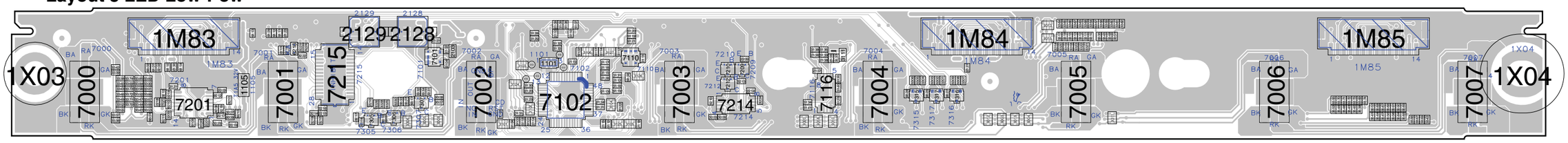
1X04 REF EMC HOLE

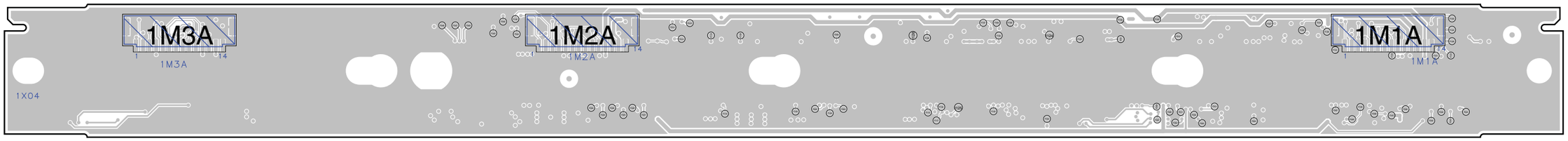
3104 313 6314.3

CHN	SETNAME		
CLASS_NO	2LED + CONNECTOR 2K9	8204 000 8874	1 2008-05-23 2 2008-08-08 3 0
2008-05-23 1 2008-08-08 2 2008-10-31 3			
NAME Peter Van Hove	SUPERS. 1	130 – 1	A2
CHECK	DATE 2008-04-20	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_653_090508.eps
090508

Layout 8 LED Low-Pow



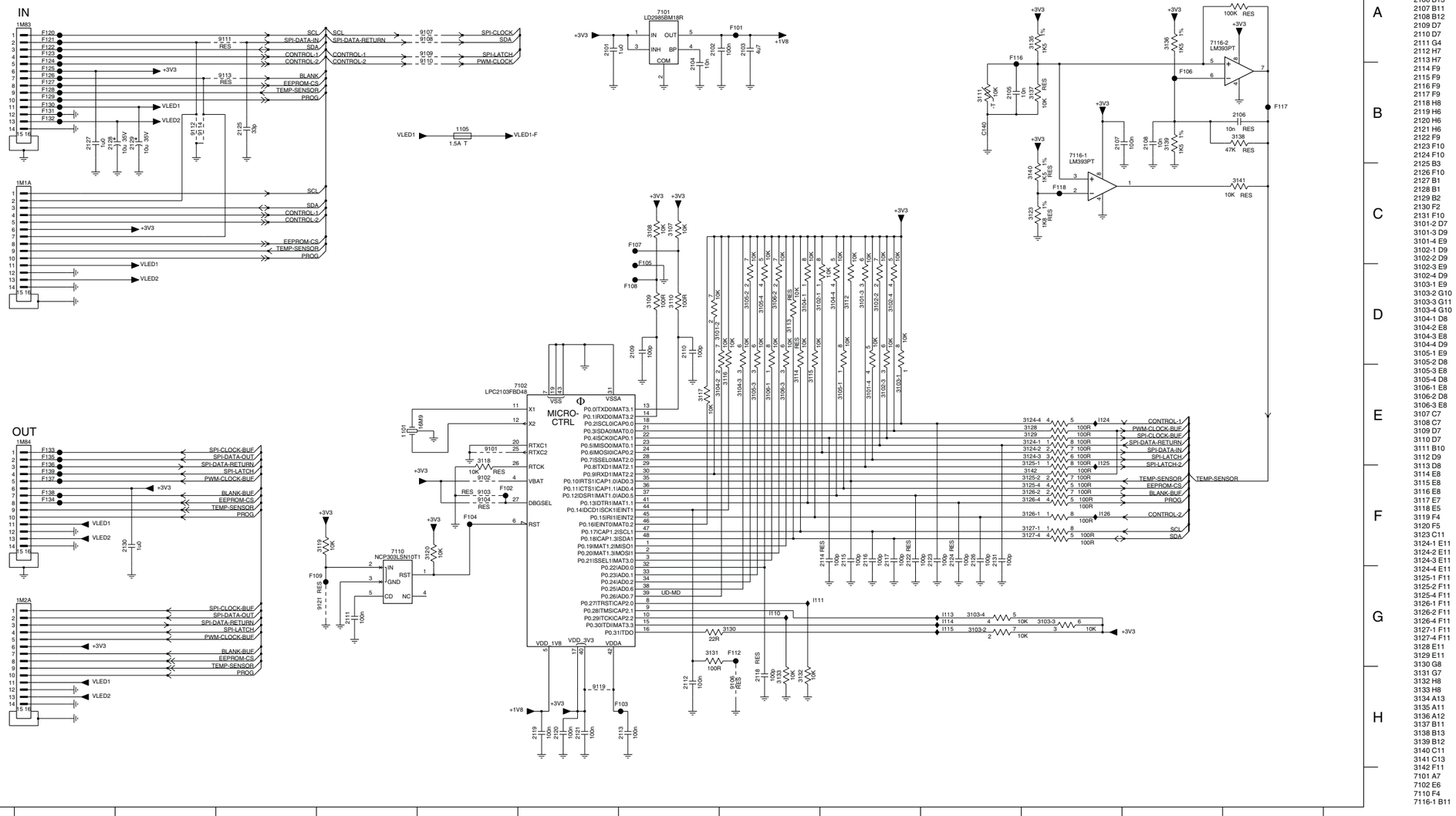


31043136314.3

18490_550_090326.eps
090326

10 LED Low-Pow: Microcontroller Block Liteon

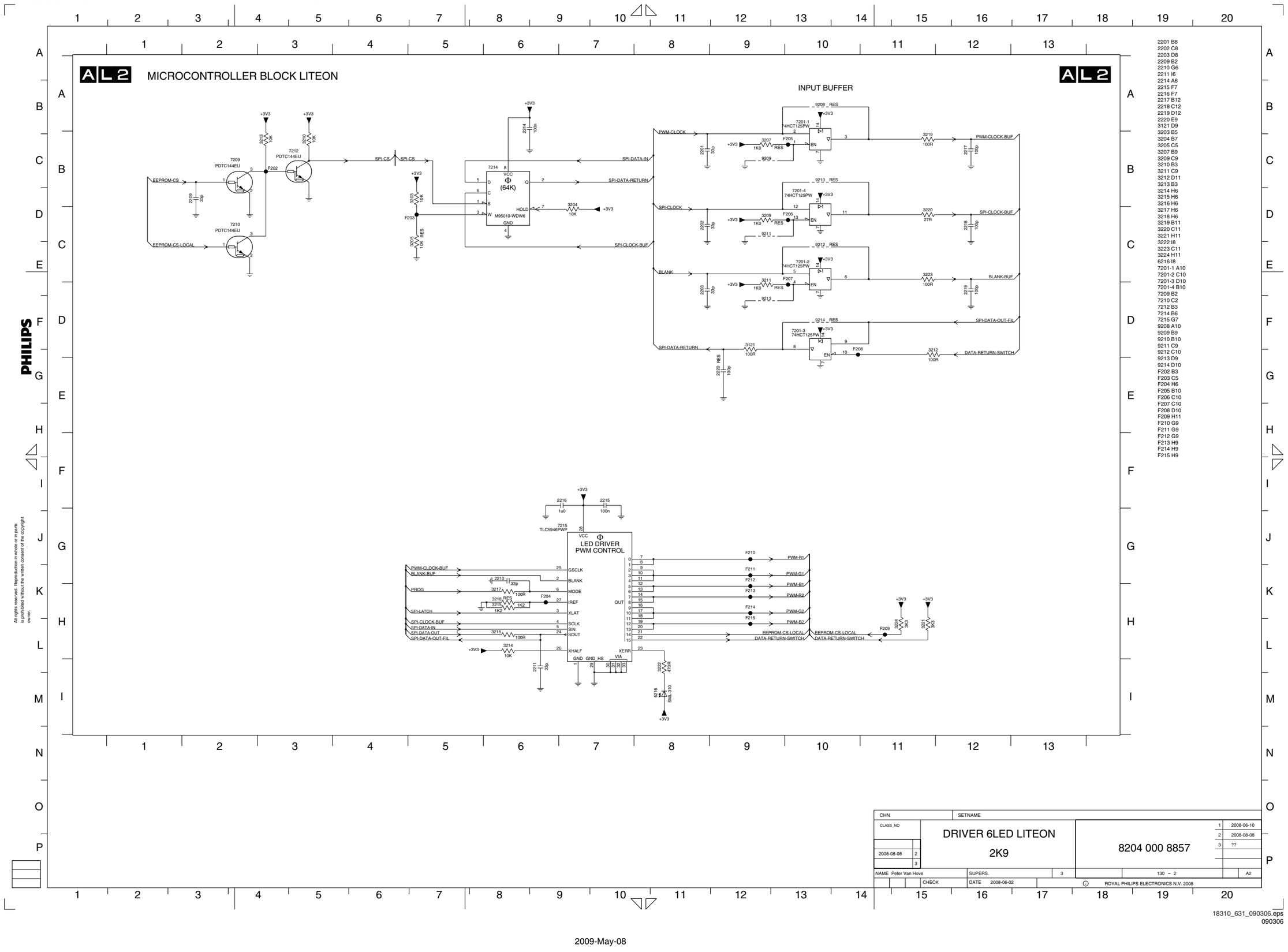
AL 1 MICROCONTROLLER BLOCK LITEON



CHN	SETNAME		
CLASS_NO	DRIVER 6LED LITEON 2K9	8204 000 8857	1 2008-06-10
2008-08-08 2 3			2 2008-08-08
			3 ??
NAME Peter Van Hove	SUPERS. 3	130 ~ 1	A2
CHECK	DATE 2008-06-02	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_630_090306.eps
090306

10 LED Low-Pow: Microcontroller Block Liteon

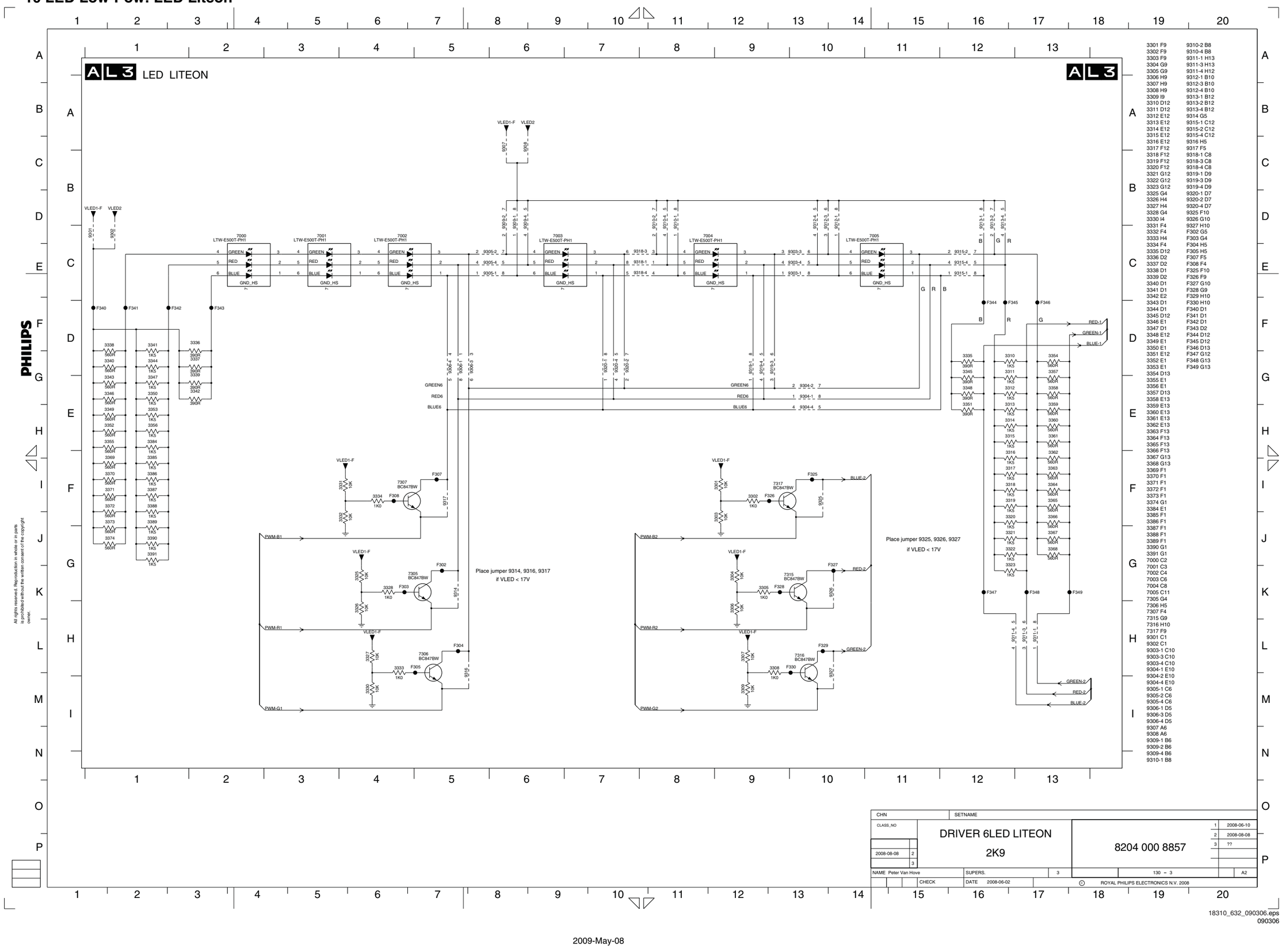


2201 B8
2202 C8
2203 D8
2209 B2
2210 G6
2211 I6
2214 A6
2215 F7
2216 F7
2217 B12
2218 C12
2219 D12
2220 E9
3121 D9
3203 B5
3204 B7
3205 C5
3207 B9
3209 C9
3210 B3
3211 C9
3212 D11
3213 B3
3214 H6
3215 H6
3216 H6
3217 H6
3218 H6
3219 B11
3220 C11
3221 H11
3222 I8
3223 C11
3224 H11
6216 I8
7201-1 A10
7201-2 C10
7201-3 D10
7201-4 B10
7209 B2
7210 C2
7212 B3
7214 B6
7215 G7
9208 A10
9209 B9
9210 B10
9211 C9
9212 C10
9213 D9
9214 D10
F202 B3
F203 C5
F204 H6
F205 B10
F206 C10
F207 C10
F208 D10
F209 H11
F210 G9
F211 G9
F212 G9
F213 H9
F214 H9
F215 H9

CHN	SETNAME		
CLASS_NO	DRIVER 6LED LITEON 2K9	8204 000 8857	1 2008-06-10 2 2008-08-08 3 ??
2008-08-08 2 3			
NAME Peter Van Hove	SUPERS. 3	130 – 2	A2
CHECK	DATE 2008-06-02	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_631_090306.eps
090306

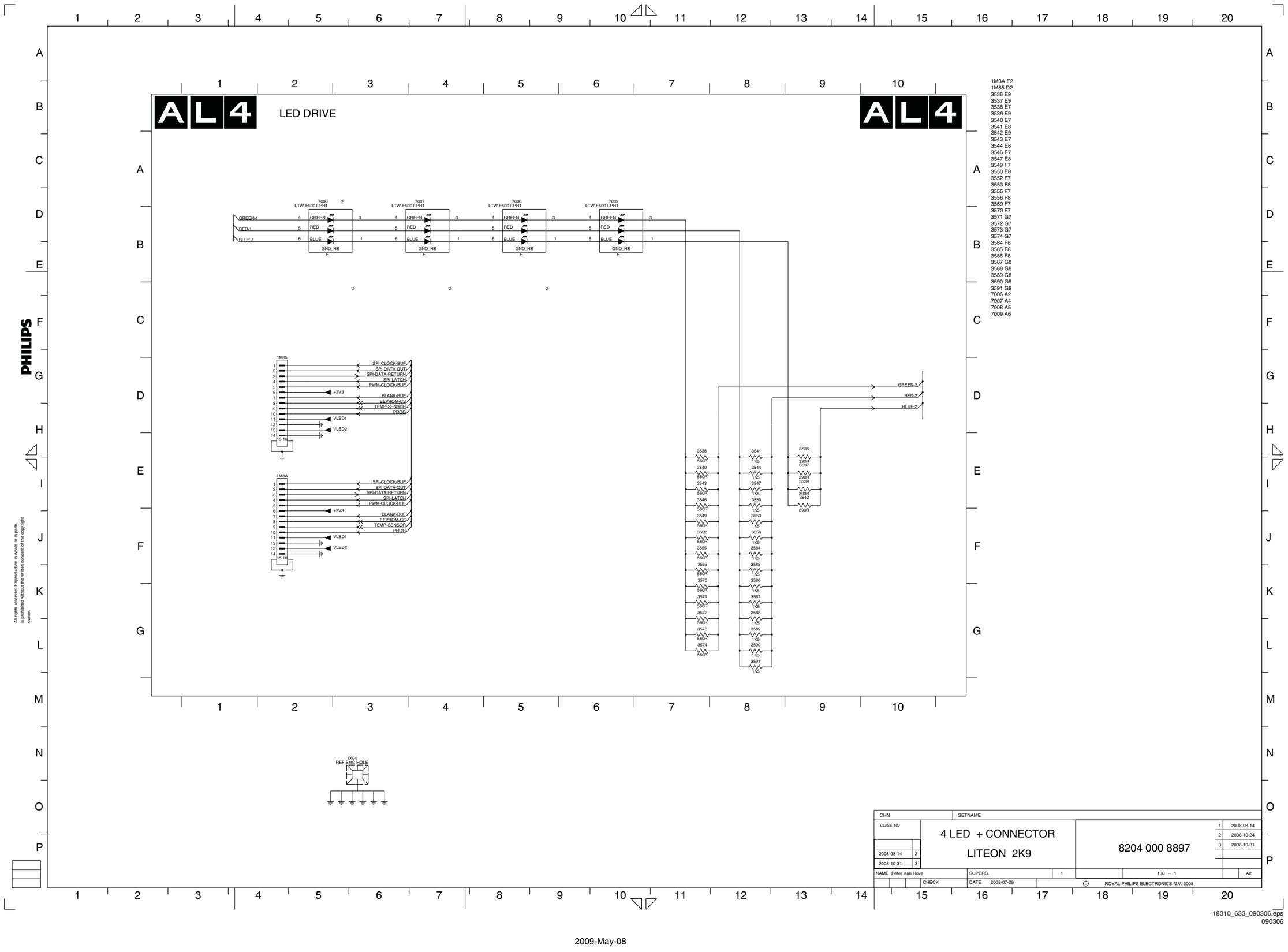
10 LED Low-Pow: LED Liteon



CHN	SETNAME		
CLASS_NO	DRIVER 6LED LITEON 2K9	8204 000 8857	1 2008-06-10
2008-08-08 2			2 2008-08-08
3			3 ??
NAME Peter Van Hove	SUPERS. 3	130 ~ 3	A2
CHECK	DATE 2008-06-02	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_632_090306.eps
090306

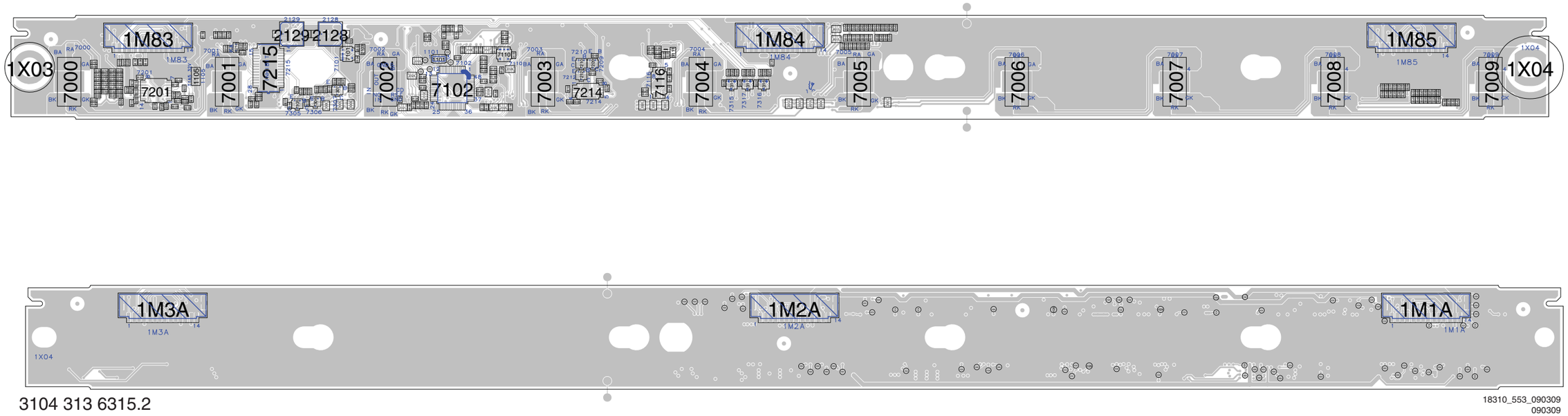
10 LED Low-Pow: LED Drive Liteon



CHN	SETNAME		
CLASS_NO	4 LED + CONNECTOR LITEON 2K9	8204 000 8897	1 2008-08-14 2 2008-10-24 3 2008-10-31
2008-08-14 2 2008-10-31 3			
NAME Peter Van Hove	SUPERS. 1	130 - 1	A2
CHECK	DATE 2008-07-29	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_633_090306.eps
090306

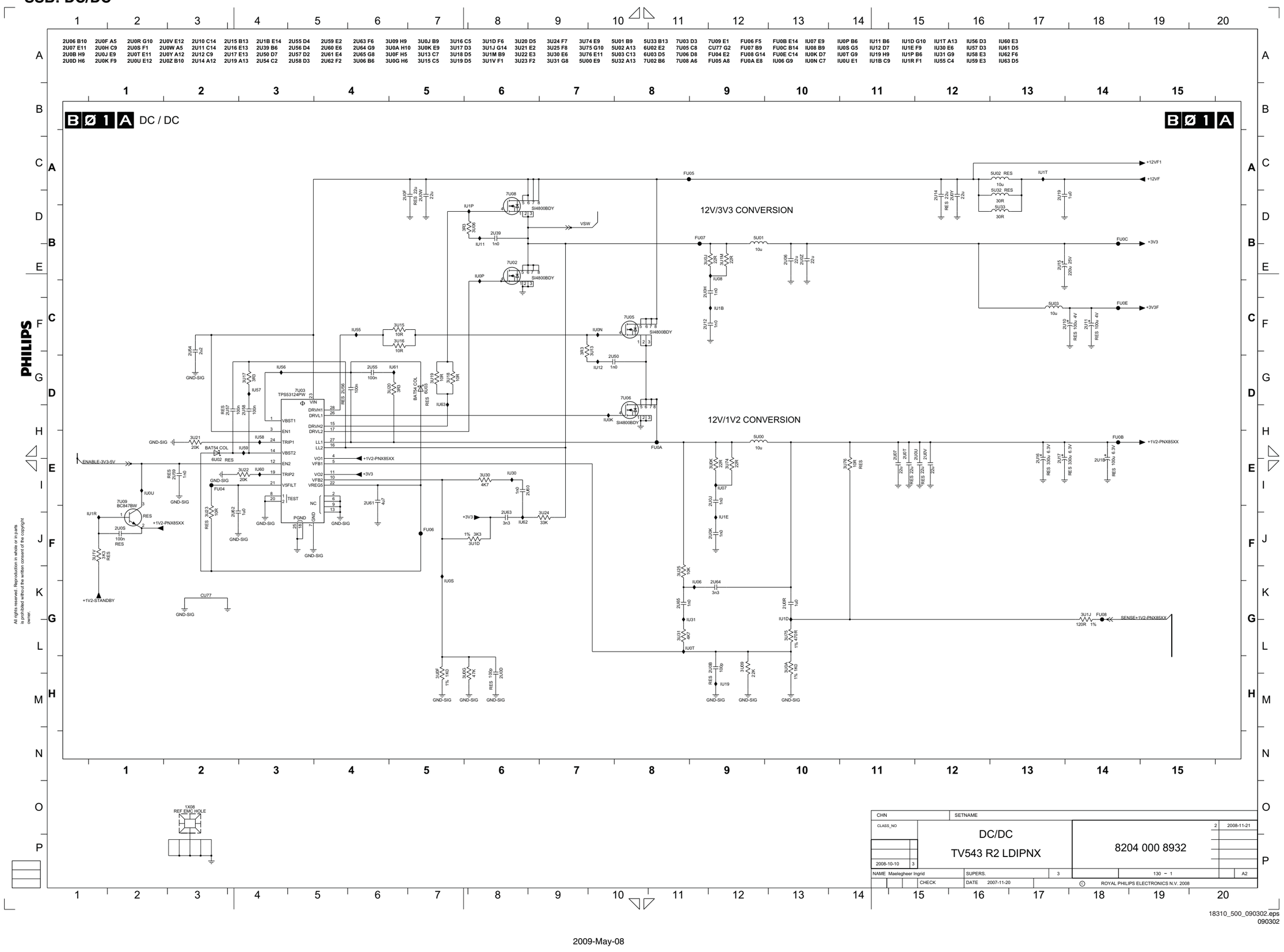
Layout 10 LED Low-Pow



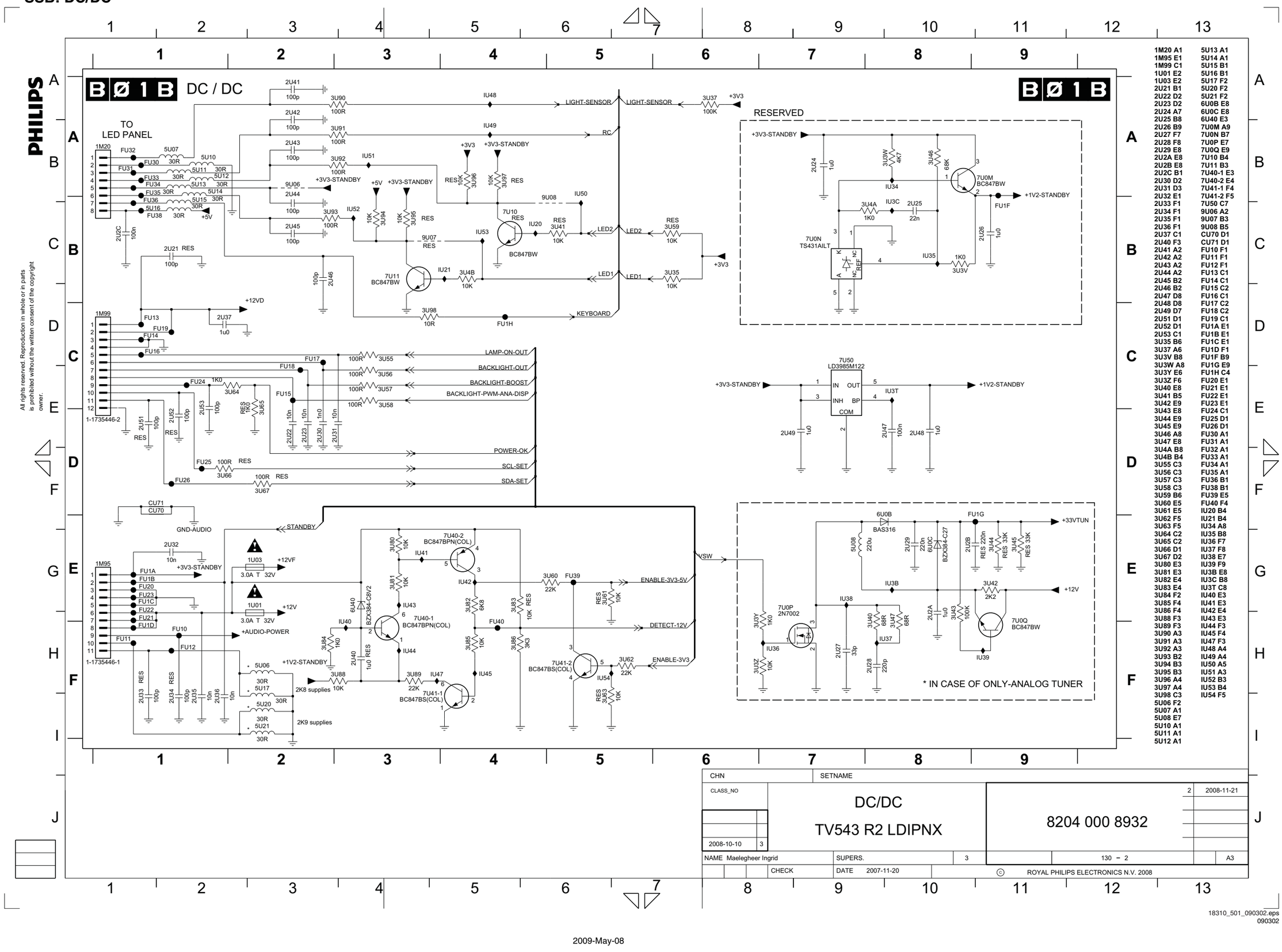
3104 313 6315.2

18310_553_090309
090309

SSB: DC/DC



SSB: DC/DC



1M20 A1	5U13 A1	2U41 B4	3U55 C3
1M95 E1	5U14 A1	2U42 B4	3U56 C3
1M99 C1	5U15 B1	2U43 B4	3U57 C3
1U01 E2	5U16 B1	2U44 B4	3U58 C3
1U03 E2	5U17 F2	2U45 B4	3U59 B6
2U21 B1	5U20 F2	2U46 B4	3U60 E5
2U22 D2	5U21 F2	2U47 D8	3U61 E5
2U23 D2	6U0B E8	2U48 D8	3U62 F5
2U24 A7	6U0C E8	2U49 D7	3U63 F5
2U25 B8	6U40 E3	2U51 D1	3U64 C2
2U26 B9	7U0M A9	2U52 D1	3U65 C2
2U27 F7	7U0N B7	2U53 C1	3U66 B6
2U28 F8	7U0P E7	3U35 B6	3U67 D2
2U29 E8	7U0Q E9	3U37 A6	3U80 E3
2U2A E8	7U10 B4	3U3V B8	3U81 E3
2U2B E8	7U11 B3	3U3W A8	3U82 E4
2U2C B1	7U40-1 E3	3U3Y E6	3U84 F2
2U30 D2	7U40-2 E4	3U3Z F6	3U85 F4
2U31 D3	7U41-1 F4	3U40 E8	3U86 F4
2U32 E1	7U41-2 F5	3U41 B5	3U88 F3
2U33 F1	7U50 C7	3U42 E9	3U89 F3
2U34 F1	9U06 A2	3U43 E8	3U90 A3
2U35 F1	9U07 B3	3U44 E9	3U91 A3
2U36 F1	9U08 B5	3U45 E9	3U92 A3
2U37 C1	CU70 D1	3U46 A8	3U93 B2
2U40 F3	CU71 D1	3U47 E8	3U94 B3
2U41 A2	FU10 F1	3U4A B8	3U95 B3
2U42 A2	FU11 F1	3U4B B4	3U96 A4
2U43 A2	FU12 F1	3U55 C3	3U97 A4
2U44 A2	FU13 C1	3U56 C3	3U98 C3
2U45 B2	FU14 C1	3U57 C3	5U06 F2
2U46 B2	FU15 C2	3U58 C3	5U07 A1
2U47 D8	FU16 C1	3U59 B6	5U08 E7
2U48 D8	FU17 C2	3U60 E5	5U10 A1
2U49 D7	FU18 C2	3U61 E5	5U11 A1
2U51 D1	FU19 C1	3U62 F5	5U12 A1
2U52 D1	FU1A E1	3U63 F5	
2U53 C1	FU1B E1	3U64 C2	
3U35 B6	FU1C E1	3U65 C2	
3U37 A6	FU1D F1	3U66 B6	
3U3V B8	FU1F B9	3U67 D2	
3U3W A8	FU1G E9	3U80 E3	
3U3Y E6	FU1H C4	3U81 E3	
3U3Z F6	FU20 E1	3U82 E4	
3U40 E8	FU21 E1	3U84 F2	
3U41 B5	FU22 E1	3U85 F4	
3U42 E9	FU23 E1	3U86 F4	
3U43 E8	FU24 C1	3U88 F3	
3U44 E9	FU25 D1	3U89 F3	
3U45 E9	FU26 D1	3U90 A3	
3U46 A8	FU30 A1	3U91 A3	
3U47 E8	FU31 A1	3U92 A3	
3U4A B8	FU32 A1	3U93 B2	
3U4B B4	FU33 A1	3U94 B3	
3U55 C3	FU34 A1	3U95 B3	
3U56 C3	FU35 A1	3U96 A4	
3U57 C3	FU36 B1	3U97 A4	
3U58 C3	FU38 B1	3U98 C3	
3U59 B6	FU39 E5	5U06 F2	
3U60 E5	FU40 F4	5U07 A1	
3U61 E5	IU20 B4	5U08 E7	
3U62 F5	IU21 B4	5U10 A1	
3U63 F5	IU34 A8	5U11 A1	
3U64 C2	IU35 B8	5U12 A1	
3U65 C2	IU36 F7		
3U66 D1	IU37 F8		
3U67 D2	IU38 E7		
3U80 E3	IU39 F9		
3U81 E3	IU3B E8		
3U82 E4	IU3C B8		
3U83 E4	IU3T C8		
3U84 F2	IU40 E3		
3U85 F4	IU41 E3		
3U86 F4	IU42 E4		
3U88 F3	IU43 E3		
3U89 F3	IU44 F3		
3U90 A3	IU45 F4		
3U91 A3	IU47 F3		
3U92 A3	IU48 A4		
3U93 B2	IU49 A4		
3U94 B3	IU50 A5		
3U95 B3	IU51 A3		
3U96 A4	IU52 B3		
3U97 A4	IU53 B4		
3U98 C3	IU54 F5		
5U06 F2			
5U07 A1			
5U08 E7			
5U10 A1			
5U11 A1			
5U12 A1			

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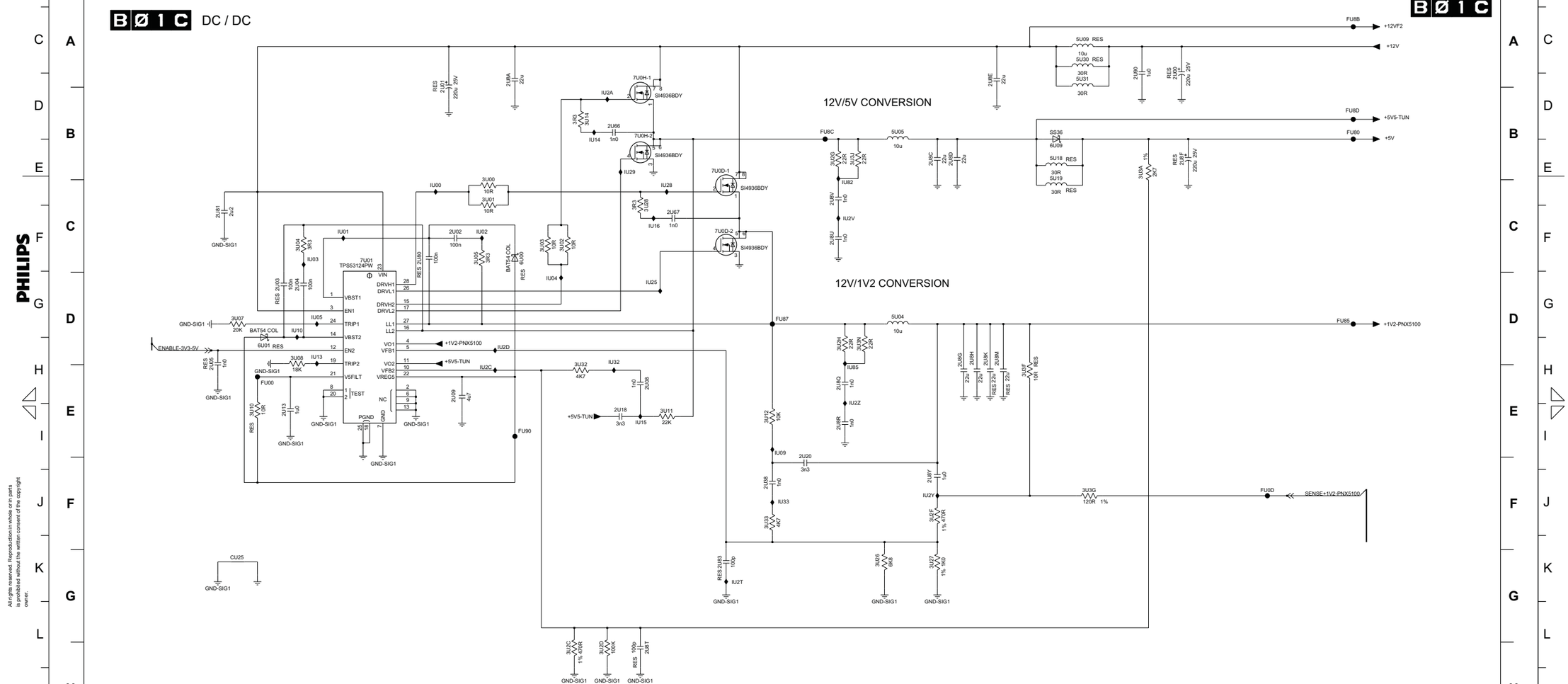
090302

SSB: DC/DC

2U00 A12 2U01 A4 2U02 C4 2U03 D2 2U04 D3 2U05 D2 2U08 E6 2U09 E4 2U13 E3 2U18 E6 2U20 F8 2U38 F8 2U66 B6 2U67 C7 2U80 C4 2U81 C2 2U83 G7 2U8A A5 2U8C B10 2U8D B10 2U8E A10 2U8F B12 2U8G D10 2U8H D10 2U8K D10 2U8M D10 2U8Q E9 2U8R E9 2U8T H6 2U8U C8 2U8V C8 2U8Y F9 2U90 A12 3U00 C5 3U01 C5 3U02 C6 3U03 C5 3U04 C3 3U05 C5 3U07 D2 3U08 D3 3U10 E2 3U11 E7 3U12 E8 3U14 B6 3U26 G9 3U27 G10 3U28 C6 3U2C H6 3U2D H6 3U2F F10 3U2G B8 3U2H D9 3U32 E6 3U33 F8 3U3A B12 3U3F E11 3U3G F11 3U3J B9 3U3N D9 5U04 D9 5U05 B9 5U09 A11 5U18 B11 5U19 C11 5U30 A11 5U31 A11 6U00 C5 6U01 D2 6U09 B11 7U01 C3 7U0D-1 B7 7U0D-2 C7 7U0H-1 A6 7U0H-2 B6 CU25 G2 FU00 E2 FU0D F13 FU80 B14 FU85 D14 FU87 B8 FU8B A14 FU8C B8 FU8D B14 FU90 E5 IU00 C4 IU01 C3 IU02 C5 IU03 C5 IU04 D5 IU05 D3 IU09 E8 IU10 D3 IU13 D3 IU14 B6 IU15 E6 IU16 C7 IU25 D6 IU28 C7 IU29 B6 IU2A B6 IU2C E5 IU2D D5 IU2T G7 IU2V C9 IU2Y F9 IU2Z E9 IU32 D6 IU33 F8 IU85 E9

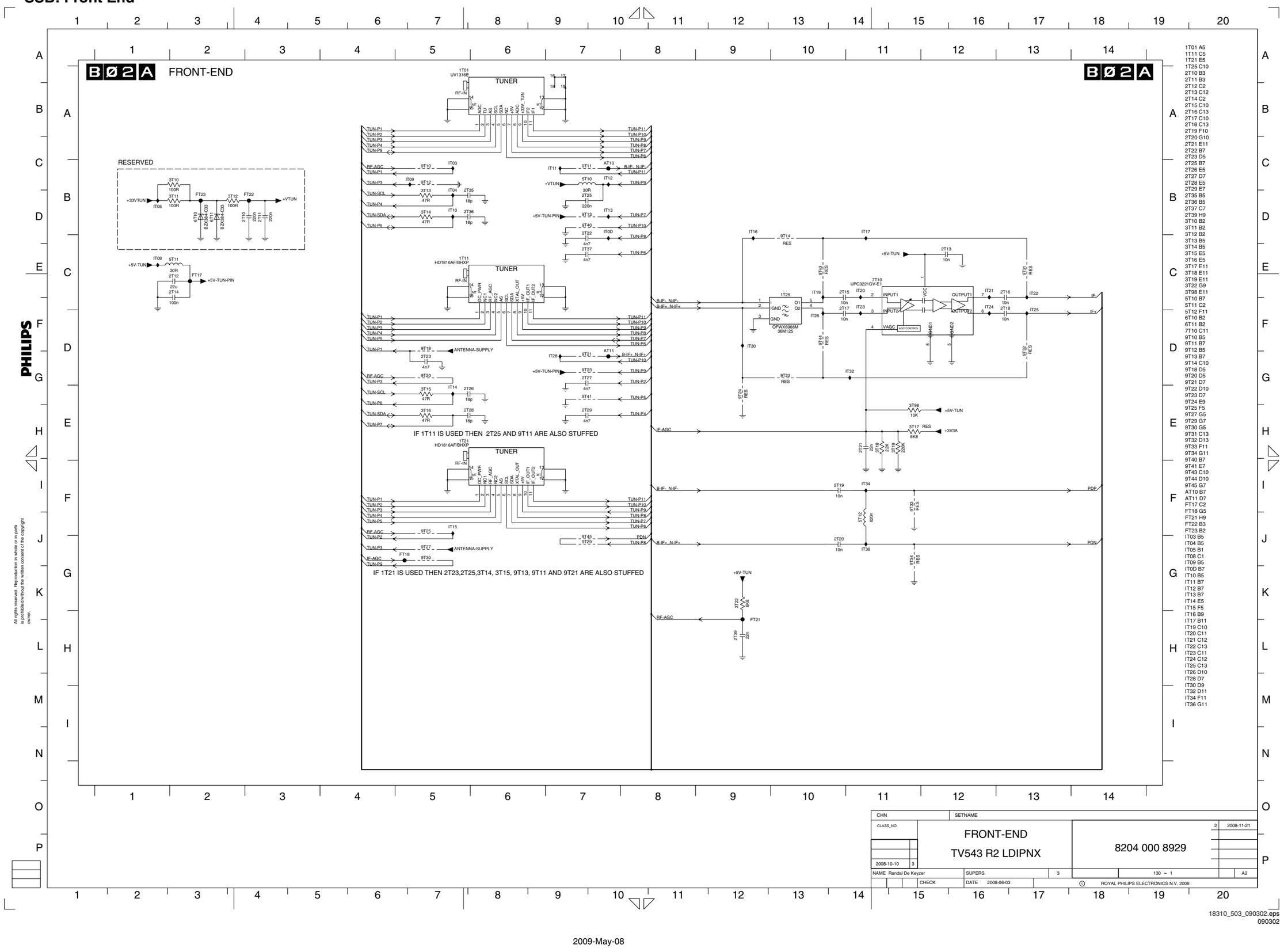
BØ1C DC / DC



CHN	SETNAME		
CLASS_NO	DC/DC TV543 R2 LDIPNX	8204 000 8932	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 3	130 ~ 3	A2
CHECK	DATE 2007-11-20	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_502_090302.eps
090302

SSB: Front End



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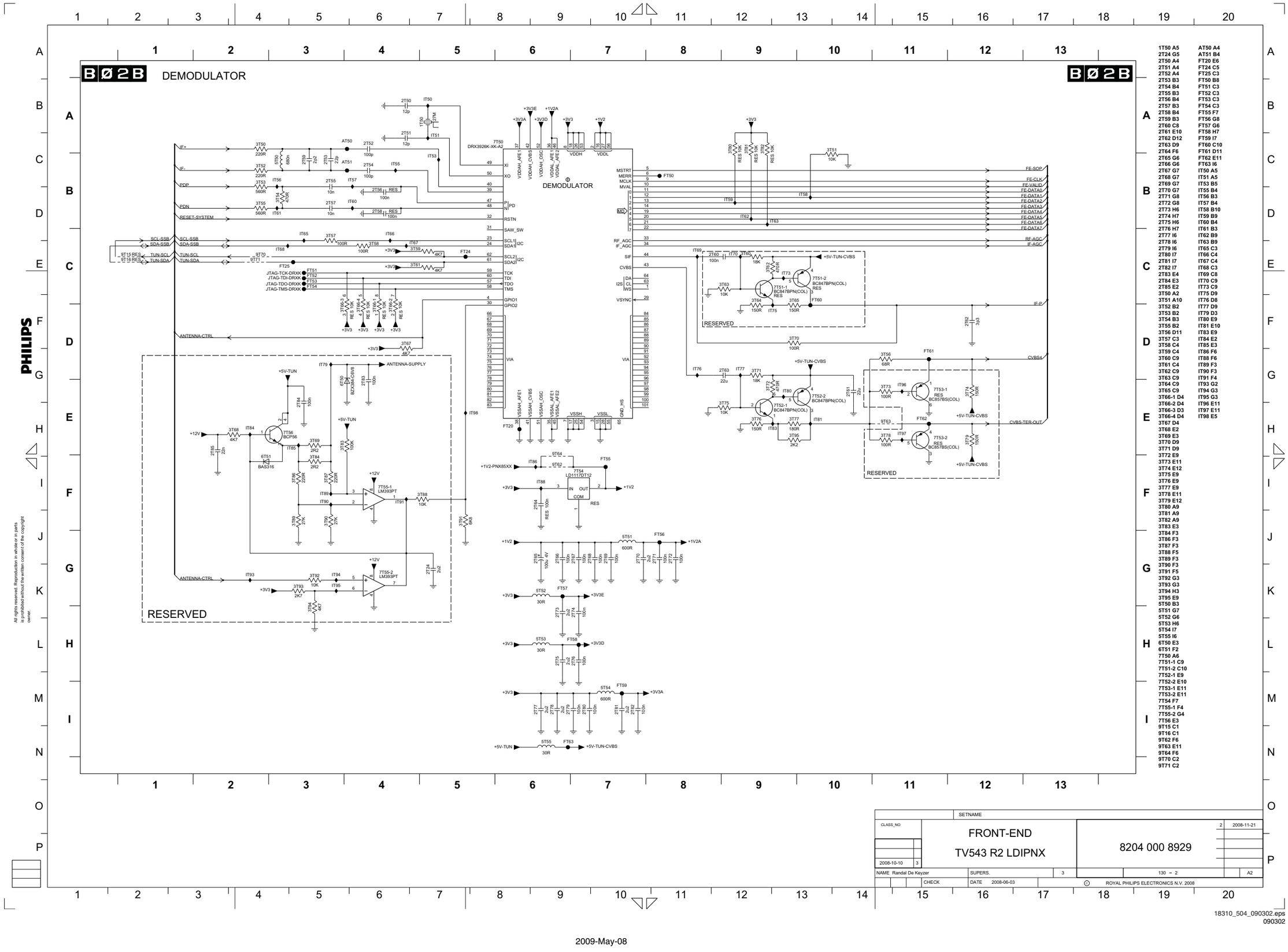
SSB: Demodulator



1T50 A5 2T24 G5 2T50 A4 2T51 A4 2T52 A4 2T53 B3 2T54 B4 2T55 B3 2T56 B4 2T57 B3 2T58 B4 2T59 B3 2T60 C8 2T61 E10 2T62 D12 2T63 D9 2T64 F6 2T65 G6 2T66 G6 2T67 G7 2T68 G7 2T69 G7 2T70 G7 2T71 G8 2T72 G8 2T73 H6 2T74 H7 2T75 H6 2T76 H7 2T77 I6 2T78 I6 2T79 I6 2T80 I7 2T81 I7 2T82 I7 2T83 E4 2T84 E3 2T85 E2 3T50 A2 3T51 A10 3T52 B2 3T53 B2 3T54 B3 3T55 B2 3T56 D11 3T57 C3 3T58 C4 3T59 C4 3T60 C9 3T61 C4 3T62 C9 3T63 C9 3T64 C9 3T65 C9 3T66-1 D4 3T66-2 D4 3T66-3 D3 3T66-4 D4 3T67 D4 3T68 E2 3T69 E3 3T70 D9 3T71 D9 3T72 E9 3T73 E11 3T74 E12 3T75 E9 3T76 E9 3T77 E9 3T78 E11 3T79 E12 3T80 A9 3T81 A9 3T82 A9 3T83 E3 3T84 F3 3T86 F3 3T87 F3 3T88 F5 3T89 F3 3T90 F3 3T91 F5 3T92 G3 3T93 G3 3T94 H3 3T95 E9 5T50 B3 5T51 G7 5T52 G6 5T53 H6 5T54 I7 5T55 I6 6T50 E3 6T51 F2 7T50 A6 7T51-1 C9 7T51-2 C10 7T52-1 E9 7T52-2 E10 7T53-1 E11 7T53-2 E11 7T54 F7 7T55-1 F4 7T55-2 G4 7T56 E3 9T15 C1 9T16 C1 9T62 F6 9T63 E11 9T64 F6 9T70 C2 9T71 C2

AT50 A4 AT51 B4 FT20 E6 FT24 C5 FT25 C3 FT50 B8 FT51 C3 FT52 C3 FT53 C3 FT54 C3 FT55 F7 FT56 G8 FT57 G6 FT58 H7 FT59 I7 FT60 C10 FT61 D11 FT62 E11 FT63 I6 IT50 A5 IT51 A5 IT53 B5 IT55 B4 IT56 B3 IT57 B4 IT58 B10 IT59 B9 IT60 B4 IT61 B3 IT62 B9 IT63 B9 IT65 C3 IT66 C4 IT67 C4 IT68 C3 IT69 C8 IT70 C9 IT73 C9 IT75 D9 IT76 D8 IT77 D9 IT79 D3 IT80 E9 IT81 E10 IT83 E9 IT84 E2 IT85 E3 IT86 F6 IT88 F6 IT89 F3 IT90 F3 IT91 F4 IT93 G2 IT94 G3 IT95 G3 IT96 E11 IT97 E11 IT98 E5

SSB: PNX8543 - Stand-by Controller

B Ø 4 A

PNX 8543 : STANDBY CONTROLLER

B Ø 4 A

PHILIPS

1HF0 A4
2H00 C3
2H01 E3
2H03 F6
2H10 D11
2H11 H7
2H12 H6
2HC0 H13
2HD0 F12
2HF0 A3
2HF1 B3
3H00 E2
3H01 E2
3H02 B11
3H03 B11
3H04 B11
3H05 B11
3H06 C11
3H07 C11
3H08 C11
3H10 B2
3H12 C12
3H13 B1
3H14 B2
3H15 B1
3H16 B2
3H17 B1
3H19 B2
3H20 C1
3H21 C2
3H22 C13
3H23 C1
3H24 C2
3H25 C13
3H26 C1
3H27 C2
3H28 C1
3H30 D2
3H31 D1
3H32 B11
3H36 D2
3H39 C2
3H41 H6
3H42 C1
3H43 H7
3H44 I4
3H46 C2
3H48 C1
3H51 C2
3H52 I13
3H53 I13
3H54 C7
3H56 C7
3H58 D2
3H60 D1
3H64 D2
3H65 B7
3H66 B7
3H67 B7
3H68 B7
3H69 C7
3H70 E2
3H72 G7
3H78-1 E6
3H78-2 E5
3H78-3 H4
3H78-4 H4
3H86-1 F4
3H86-2 F4
3H86-3 F3
3H86-4 F2
3H87-1 I2
3H87-2 I3
3H87-3 I3
3H87-4 I4
3H92-1 G4
3H92-2 G4
3H92-3 G3
3H92-4 H3
3HC2-1 H12
3HC2-2 G12
3HC2-3 H12
3HC2-4 H13
3HD4 E13
6H10 H7
6HW2 F5
7H00-6 A5
7H02 D10
7H03 C13
7H11 H8
7H14 F6
7H16-1 F5
7H16-2 G5
7H93-1 H5
7H93-2 I5
7HC3 H12
7HC4 H12
7HD0 E12
9H05 D13
9H13 G8
9H14 E11
9H15 F11
9H25 E3
9H26 E3
9H27 E3
9H28 H13
FH09 H12
FHC1 H13
FHC2 I14
FHC3 C5
FHC6 H11
FHC7 I13
FHD0 E13
FHD1 F11
FHD2 D13
IH00 D10
IH01 D11
IH02 D3
IH03 D10
IH04 G4
IH06 D10
IH07 D10
IH08 H5
IH09 C13
IH14 F5
IH15 C10
IH16 F5
IH17 G5
IH18 I4
IH19 F4
IH20 F7
IH21 I12
IH26 H4
IH32 C10
IH33 H7
IH34 G8
IH35 H7
IH36 H7
IH37 C10
IH91 H4
IH92 F9
IHC1 H12
IHC2 G12
IHD0 F12
IHW1 B4
IHW2 B4
IHW3 B4
IHW4 B4
IHW5 B5
IHW6 B4
IHW9 B4
IHWA C5
IHWB C4
IHWC C4
IHWD C4
IHWF C5
IHWG C4
IHWH C4
IHWM D4
IHWN D5

* HOTEL TV

RES

MAIN NVM

1X03 EMC HOLE

CHN	SETNAME		
CLASS_NO	STANDBY CONTROLLER PNX8543 TV543 R2 LDIPNX	8204 000 8927	2 2008-11-21
2008-10-10 3			
NAME Randal De Keyzer	SUPERS. 16	130 – 1	A2
CHECK	DATE 2007-11-29	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

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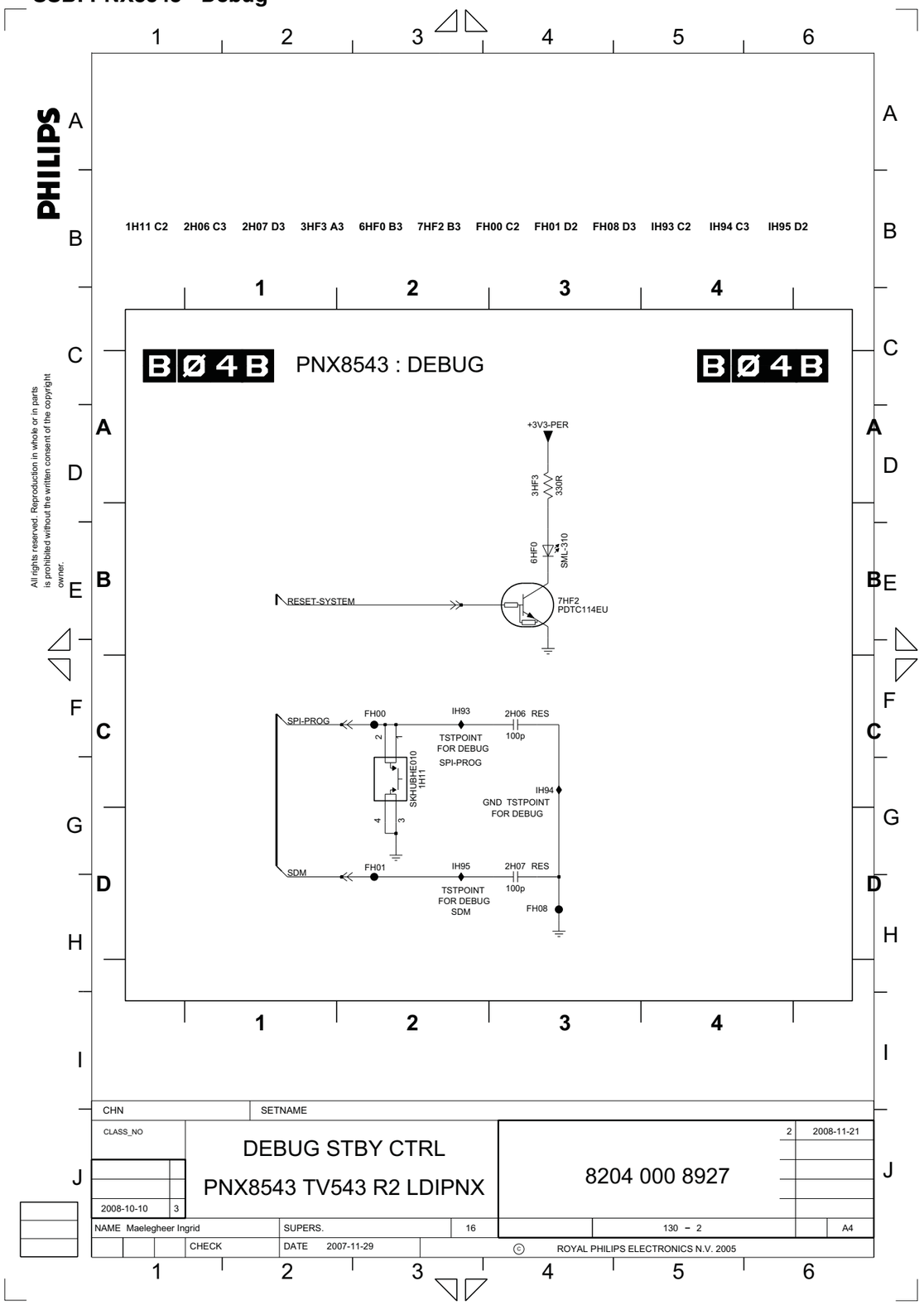
SSB: PNX8543 - Debug

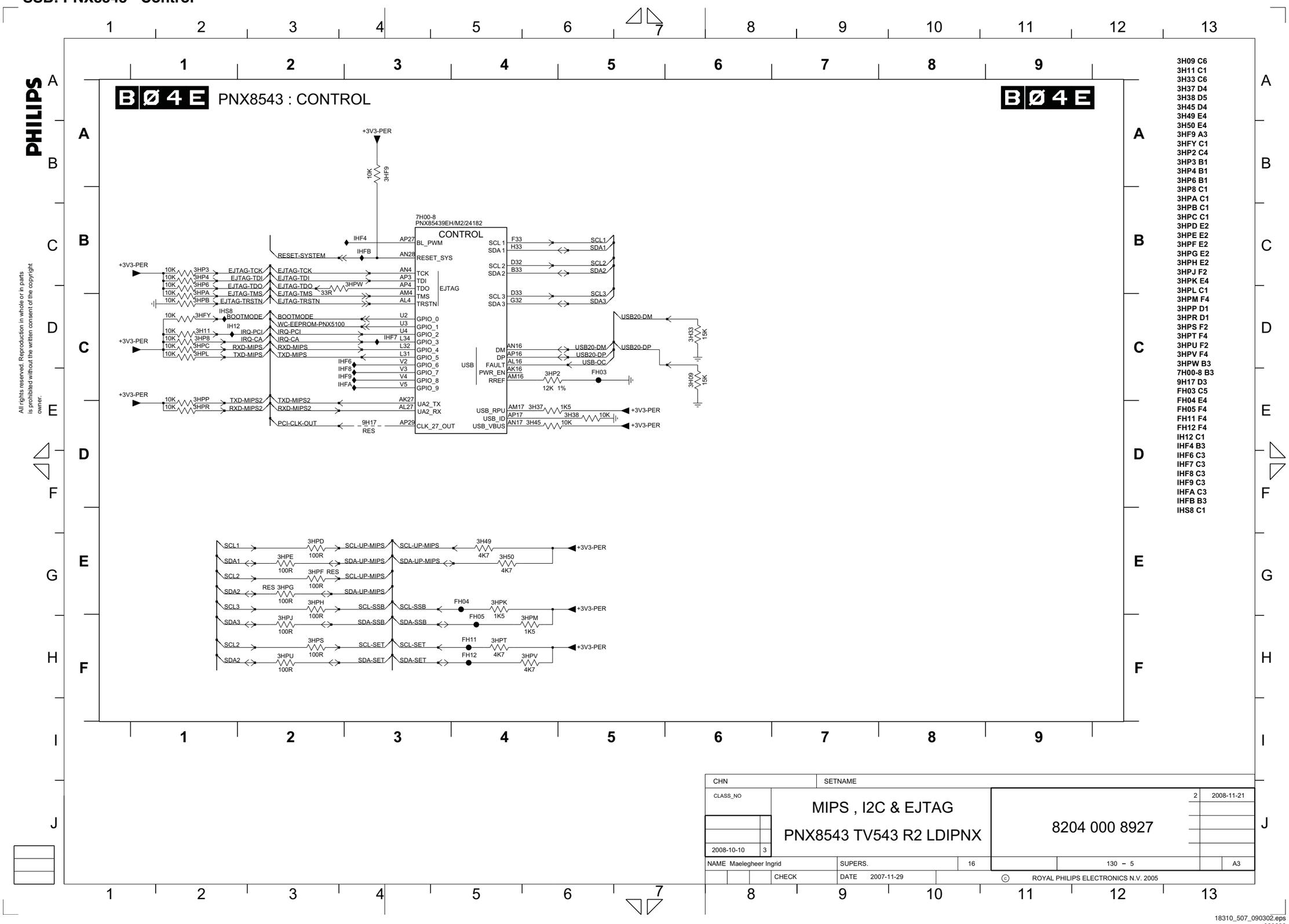


18310_506_090302.eps
090302

Personal Notes:

10000_012_090121.eps
090121

SSB: PNX8543 - Control



SSB: PNX8543 - Control

B Ø 4 F PNX 8543 : CONTROL **B Ø 4 F**

7H00-3
PNX85439EH/M2/24182

PCI

PCI_AD: PCI-AD0 … PCI-AD31 (A29, B29, C29, D29, A28, B28, C28, D28, E28, A27, B27, C27, D27, E27, A26, B26, E24, D24, C24, B24, A24, E23, D23, C23, B23, A23, E22, D22, C22, B22, A22, E21)

PCI_CBE: PCI-CBE0 (D21), PCI-CBE1 (C21), PCI-CBE2 (B21), PCI-CBE3 (A21)

CLK: PCI-CLK-PNX8535 (A30)
DEVSEL: PCI-DEVSEL (A25)
FRAME: PCI-FRAME (C26)
IDSEL: PCI-AD24 (B30) via 3HEU 100R to IH30 (C30)
INTA_OUT: PCI-IRDY (D26)
TRDY: IRDY (E25), PAR (C25), PERR (D25), SERR (B25), STOP (E26), TRDY
REQ: PCI-REQ (D30)
GNT: PCI-GNT (E30)
REQ_B: PCI-REQ-B (E31)
GNT_B: PCI-GNT-B (E29)
PLL_OUT: PCI-CLK-OUT (AP28) via IHS7, 9HG3
XIO_ACK: XIO-ACK (A20)
XIO_AD25: B19
XIO_SEL: XIO-SEL-NAND (B20) via 3HF5 100R; IHF1 (C20), IHF2 (D20), IHF3 (E20)

PCI-DEVSEL, PCI-FRAME, PCI-IRDY, PCI-TRDY, PCI-STOP, PCI-PERR, PCI-SERR: 4K7 pull-ups to +3V3-PER via 3HFD-4, 3HFD-1, 3HFD-2, 3HFD-3, 3HFE-2, 3HFE-3, 3HFE-1

PCI-REQ: 4K7 to +3V3-PER via 3HES-2 → 9HF6 → PCI-REQ-ETH
PCI-GNT: 4K7 to +3V3-PER via 3HES-3 → 9HF7 → PCI-GNT-ETH
PCI-REQ-B: 4K7 to +3V3-PER via 3HES-1 → 9HF4 → PCI-REQ-MINI
PCI-GNT-B: 4K7 to +3V3-PER via 3HES-4 → 9HF5 → PCI-GNT-MINI

PCI-CLK-OUT → 3HFG 10R → PCI-CLK-ETHERNET
IHF0 → 3HFH 10R → IHF5 → PCI-CLK-PNX5100
3HF2 10R → PCI-CLK-PNX8535
3HF4* 10R → PCI-CLK-MINI

RESERVED

PCI-CLK-OUT → 3HFR 33R → 7HF1 CY2305S ZERO DELAY BUFFER (REF, CLK, CLKOUT, VDD, GND)
+3V3-PER → 2HF5 10n, 2HF6 100n, 2HF7 10p
CLK → 3HFK 33R → PCI-CLK-PNX8535; 3HFP 33R → PCI-CLK-ETHERNET
CLKOUT → 3HFM 33R → PCI-CLK-PNX5100; 3HFN 33R → PCI-CLK-MINI

2HF5 D7
2HF6 D7
2HF7 D7
3HES-1 C5
3HES-2 B5
3HES-3 C5
3HES-4 C5
3HEU B3
3HF2 E2
3HF4 E2
3HF5 C3
3HFD-1 A6
3HFD-2 A5
3HFD-3 A6
3HFD-4 A5
3HFE-1 A6
3HFE-2 A6
3HFE-3 A6
3HFG D2
3HFH E2
3HFK E7
3HFM E7
3HFN E7
3HFP E7
3HFR E5
7H00-3 A2
7HF1 D6
9HF4 C6
9HF5 C6
9HF6 B6
9HF7 B6
9HG3 C3
IH30 B4
IHF0 E2
IHF1 C3
IHF2 C3
IHF3 D3
IHF5 E2
IHS7 C3

CHN	SETNAME		
CLASS_NO	CONTROL	2	2008-11-21
2008-10-03 2	PNX8543 TV543 R2 LDIPNX	8204 000 8927	
NAME Maelegheer Ingrid	SUPERS. 16	130 – 6	A3
CHECK	DATE 2007-11-29	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

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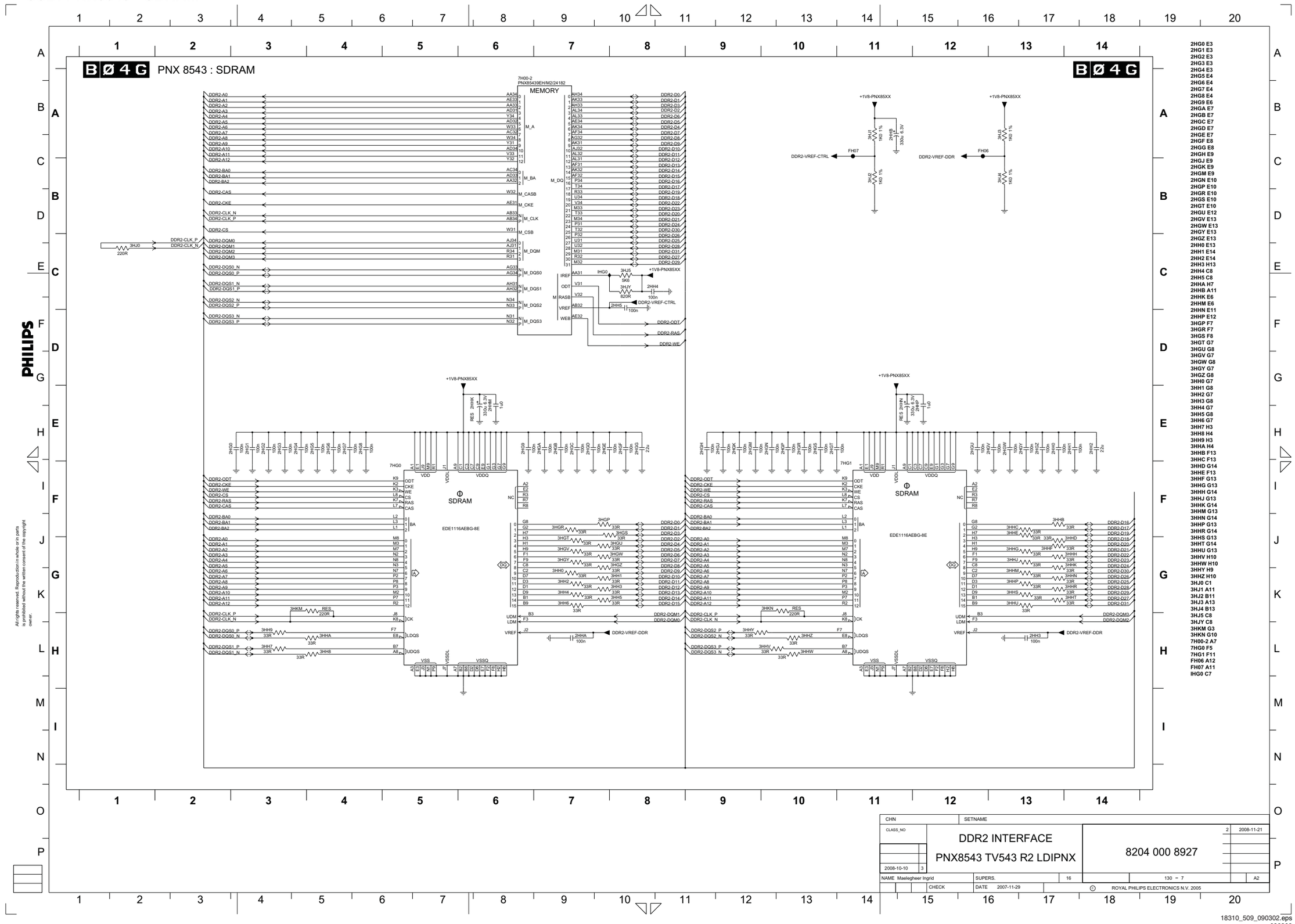
SSB: PNX8543 - SDRAM



2HG0 E3
2HG1 E3
2HG2 E3
2HG3 E3
2HG4 E3
2HG5 E4
2HG6 E4
2HG7 E4
2HG8 E4
2HG9 E6
2HGA E7
2HGB E7
2HGC E7
2HGD E7
2HGE E7
2HGF E8
2HGG E8
2HGH E9
2HGJ E9
2HGK E9
2HGM E9
2HGN E10
2HGP E10
2HGR E10
2HGS E10
2HGT E10
2HGU E12
2HGV E13
2HGW E13
2HGY E13
2HGZ E13
2HH0 E13
2HH1 E14
2HH2 E14
2HH3 H13
2HH4 C8
2HH5 C8
2HHA H7
2HHB A11
2HHK E6
2HHM E6
2HHN E11
2HHP E12
3HGP F7
3HGR F7
3HGS F8
3HGT G7
3HGU G8
3HGV G7
3HGW G8
3HGY G7
3HGZ G8
3HH0 G7
3HH1 G8
3HH2 G7
3HH3 G8
3HH4 G7
3HH5 G8
3HH6 G7
3HH7 H3
3HH8 H4
3HH9 H3
3HHA H4
3HHB F13
3HHC F13
3HHD G14
3HHE F13
3HHF G13
3HHG G13
3HHH G14
3HHJ G13
3HHK G14
3HHM G13
3HHN G14
3HHP G13
3HHR G14
3HHS G13
3HHT G14
3HHU G13
3HHV H10
3HHW H10
3HHY H9
3HHZ H10
3HJ0 C1
3HJ1 A11
3HJ2 B11
3HJ3 A13
3HJ4 B13
3HJ5 C8
3HJY C8
3HKM G3
3HKN G10
7H00-2 A7
7HG0 F5
7HG1 F11
FH06 A12
FH07 A11
IHG0 C7

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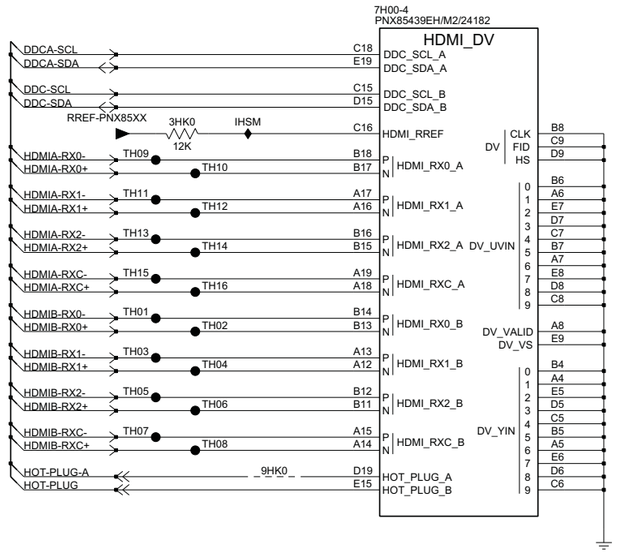
090302

SSB: PNX8543 - Digital Video In

PHILIPS

B Ø 4 H PNX 8543 : DIGITAL VIDEO IN B Ø 4 H



3HK0 B2
7H00-4 A3
9HK0 D2
IHSM B2
TH01 C2
TH02 C2
TH03 C2
TH04 C2
TH05 C2
TH06 C2
TH07 D2
TH08 D2
TH09 B2
TH10 B2
TH11 B2
TH12 B2
TH13 B2
TH14 C2
TH15 C2
TH16 C2

CHN	SETNAME		
CLASS_NO	VIDEO IN PNX8543 TV543 R2 LDIPNX	8204 000 8927	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 16	130 – 8	A3
CHECK	DATE 2007-11-29	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

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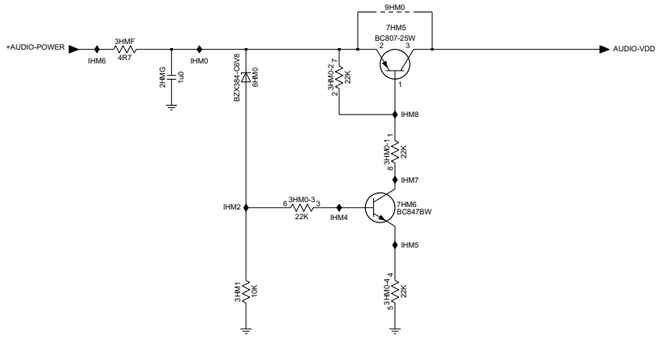
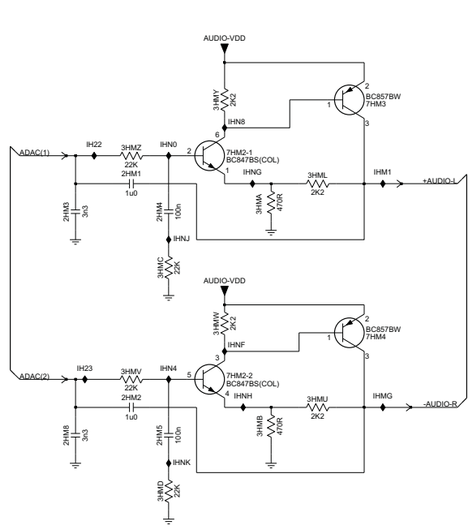
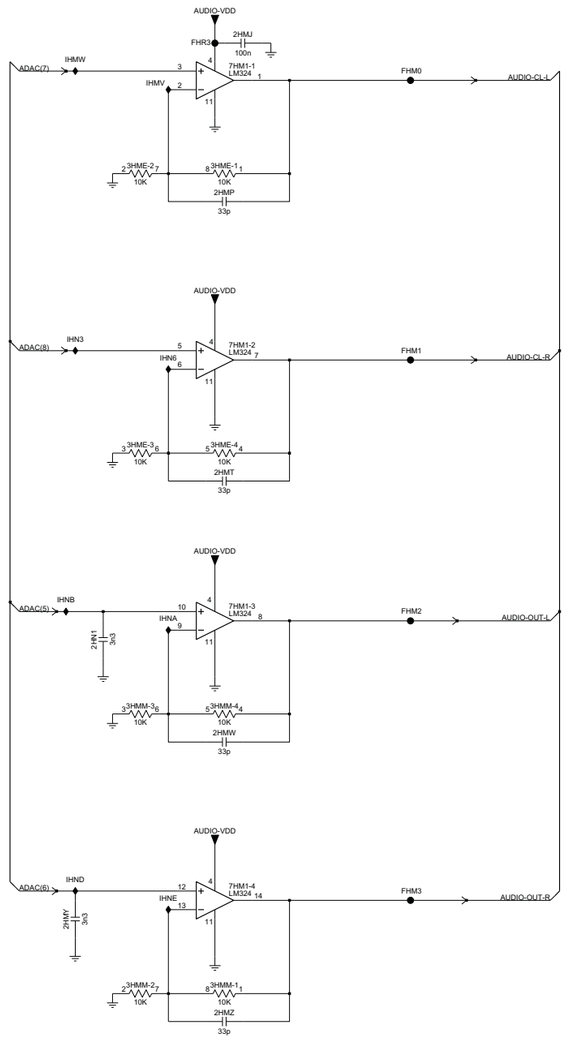
SSB: PNX8543 - Audio

B041 PNX 8543 : AUDIO







2HM1 G5
2HM2 H5
2HM3 G4
2HM4 G5
2HM5 H5
2HM8 H4
2HMG B3
2HMJ A10
2HMP C10
2HMT E10
2HMW G10
2HMY H9
2HMZ I10
2HN1 F9
3HM0-1 C5
3HM0-2 B4
3HM0-3 C4
3HM0-4 D5
3HM1 D4
3HMA G6
3HMB H6
3HMC G5
3HMD I5
3HME-1 B10
3HME-2 B9
3HME-3 E9
3HME-4 E10
3HMF B3
3HML G6
3HMM-1 I10
3HMM-2 I9
3HMM-3 G9
3HMM-4 G10
3HMU H6
3HMV H5
3HMW H5
3HMY F5
3HMZ F5
6HM0 B4
7HM1-1 B10
7HM1-2 D10
7HM1-3 F10
7HM1-4 H10
7HM2-1 F5
7HM2-2 H5
7HM3 F7
7HM4 H7
7HM5 B5
7HM6 C5
9HM0 B5
FHM0 B11
FHM1 D11
FHM2 F11
FHM3 H11
FHR3 A10
IH22 F4
IH23 H4
IHM0 B3
IHM1 F7
IHM2 C4
IHM4 C4
IHM5 D5
IHM6 B3
IHM7 C5
IHM8 C5
IHMG H7
IHMV B9
IHMW B9
IHN0 F5
IHN3 D9
IHN4 H5
IHN6 D10
IHN8 F6
IHNA F10
IHNB F9
IHND H9
IHNE H10
IHNF H6
IHNG F6
IHNH H6
IHNJ G5
IHNK I5

CHN	SETNAME		
CLASS_NO	AUDIO PNX8543 TV543 R2 LDIPNX	8204 000 8927	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 16	130 ~ 9	A2
	CHECK DATE 2007-11-29	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

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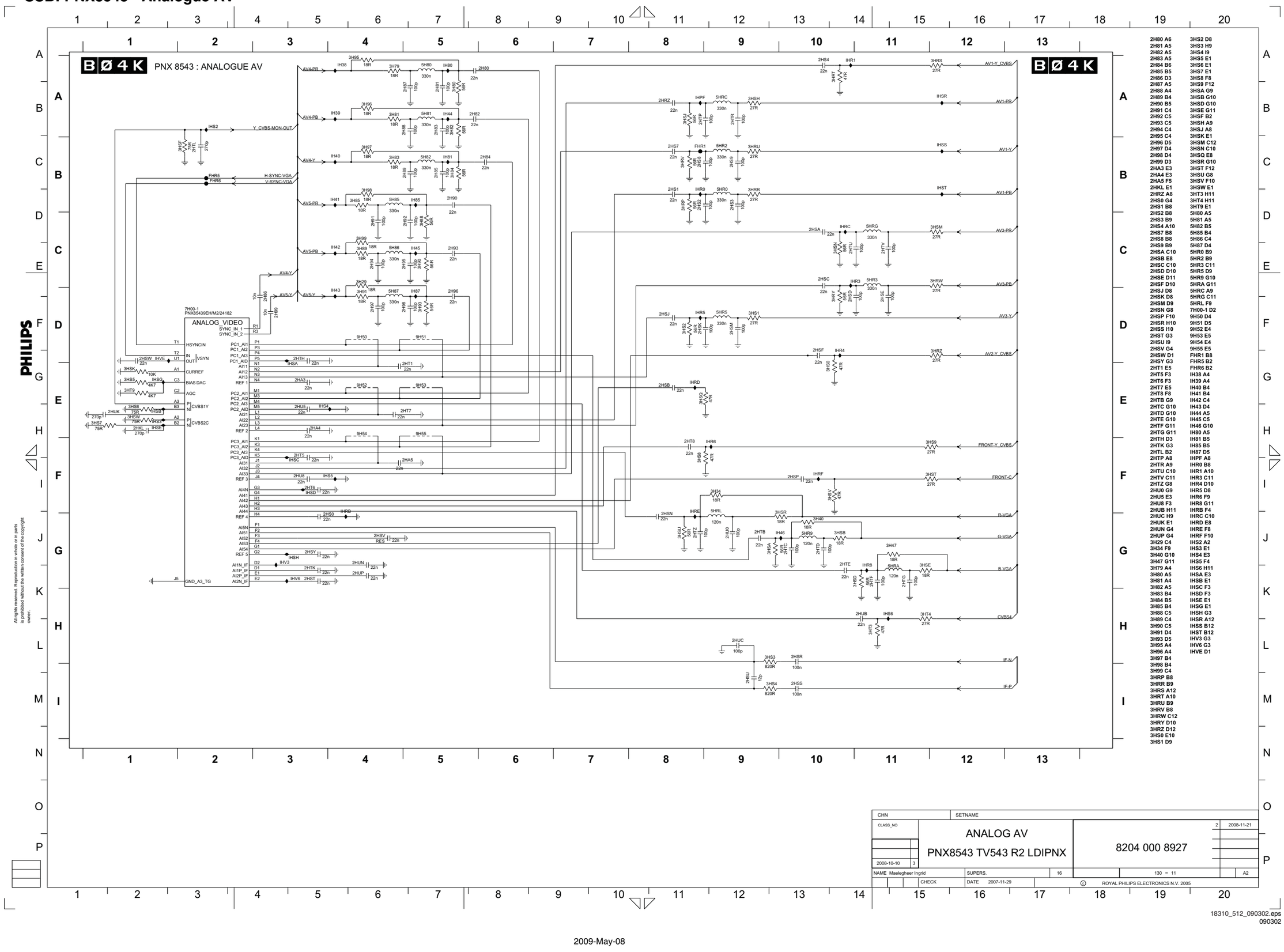
SSB: PNX8543 - Analogue AV



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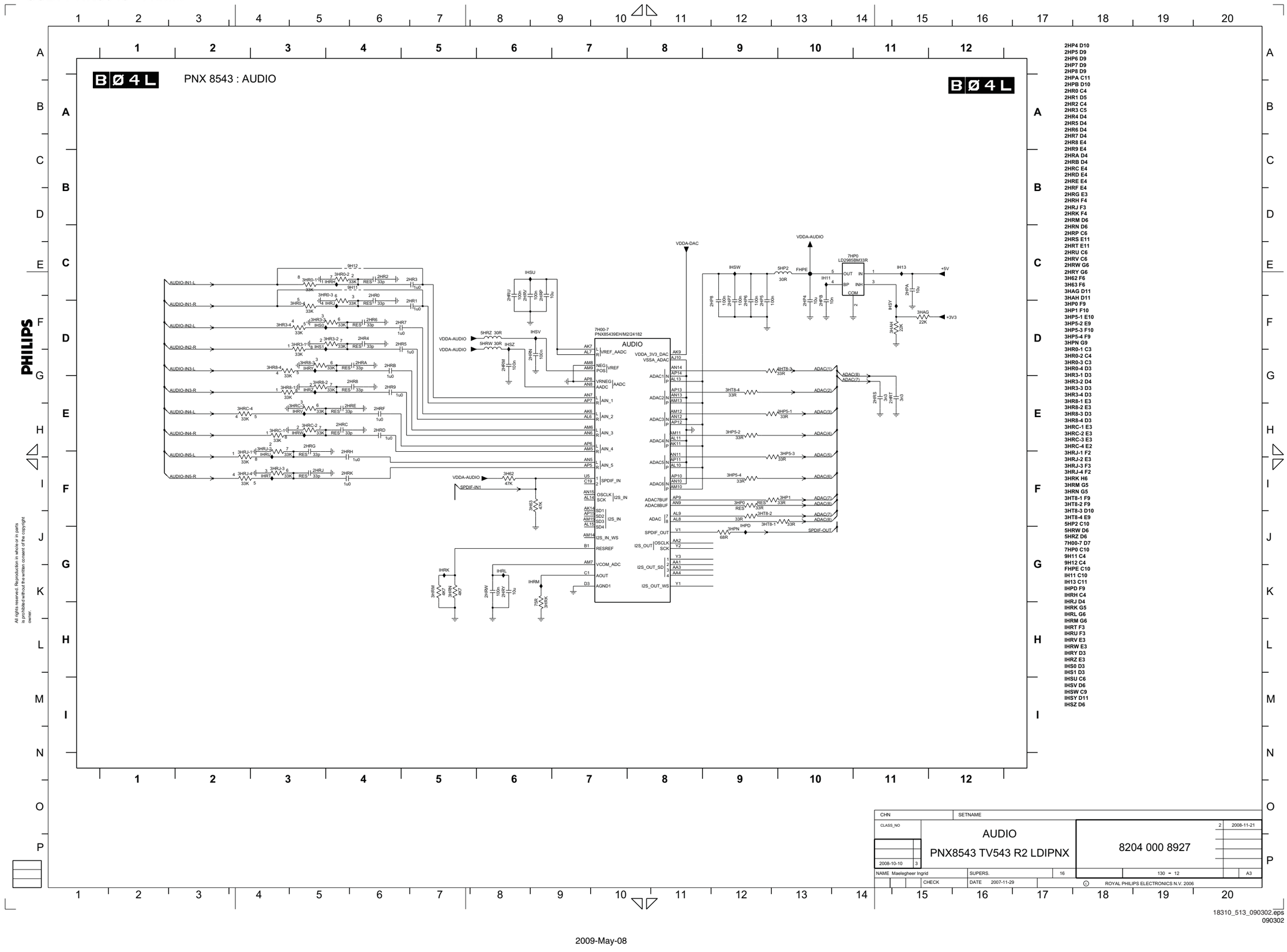
3HS2 D8 3HS3 H9 3HS4 I9 3HS5 E1 3HS6 E1 3HS7 E1 3HS8 F8 3HS9 F12 3HSA G9 3HSB G10 3HSD G10 3HSE G11 3HSF B2 3HSH A9 3HSJ A8 3HSK E1 3HSM C12 3HSN C10 3HSQ E8 3HSR G10 3HST F12 3HSU G8 3HSV F10 3HSW E1 3HT3 H11 3HT4 H11 3HT9 E1 5H80 A5 5H81 A5 5H82 B5 5H85 B4 5H86 C4 5H87 D4 5HR0 B9 5HR2 B9 5HR3 C11 5HR5 D9 5HR9 G10 5HRA G11 5HRC A9 5HRG C11 5HRL F9 7H00-1 D2 9H50 D4 9H51 D5 9H52 E4 9H53 E5 9H54 E4 9H55 E5 FHR1 B8 FHR5 B2 FHR6 B2 IH38 A4 IH39 A4 IH40 B4 IH41 B4 IH42 C4 IH43 D4 IH44 A5 IH45 C5 IH46 G10 IH80 A5 IH81 B5 IH85 B5 IH87 D5 IHPF A8 IHR0 B8 IHR1 A10 IHR3 C11 IHR4 D10 IHR5 D8 IHR6 F9 IHR8 G11 IHRB F4 IHRC C10 IHRD E8 IHRE F8 IHRF F10 IHS2 A2 IHS3 E1 IHS4 E3 IHS5 F4 IHS6 H11 IHSA E3 IHSB E1 IHSC F3 IHSD F3 IHSE E1 IHSG E1 IHSH G3 IHSR A12 IHSS B12 IHST B12 IHV3 G3 IHV6 G3 IHVE D1

SSB: PNX8543 - Audio



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2HP7 D9
2HP8 D9
2HPA C11
2HPB D10
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2HR1 D5
2HR2 C4
2HR3 C5
2HR4 D4
2HR5 D4
2HR6 D4
2HR7 D4
2HR8 E4
2HR9 E4
2HRA D4
2HRB D4
2HRC E4
2HRD E4
2HRE E4
2HRF E4
2HRG E3
2HRH F4
2HRJ F3
2HRK F4
2HRM D6
2HRN D6
2HRP C6
2HRS E11
2HRT E11
2HRU C6
2HRV C6
2HRW G6
2HRY G6
3H62 F6
3H63 F6
3HAG D11
3HAH D11
3HP0 F9
3HP1 F10
3HP5-1 E10
3HP5-2 E9
3HP5-3 F10
3HP5-4 F9
3HPN G9
3HR0-1 C3
3HR0-2 C4
3HR0-3 C3
3HR0-4 D3
3HR1-1 D3
3HR3-2 D4
3HR3-3 D3
3HR3-4 D3
3HR8-1 E3
3HR8-2 E3
3HR8-3 D3
3HR8-4 D3
3HRC-1 E3
3HRC-2 E3
3HRC-3 E3
3HRC-4 E2
3HRJ-1 F2
3HRJ-2 E3
3HRJ-3 F3
3HRJ-4 F2
3HRK H6
3HRM G5
3HRN G5
3HT8-1 F9
3HT8-2 F9
3HT8-3 D10
3HT8-4 E9
5HP2 C10
5HRW D6
5HRZ D6
7H00-7 D7
7HP0 C10
9H11 C4
9H12 C4
FHPE C10
IH11 C10
IH13 C11
IHPD F9
IHRH C4
IHRJ D4
IHRK G5
IHRL G6
IHRM G6
IHRT F3
IHRU F3
IHRV E3
IHRW E3
IHRY D3
IHRZ E3
IHS0 D3
IHS1 D3
IHSU C6
IHSV D6
IHSW C9
IHSY D11
IHSZ D6

SSB: PNX8543 - Audio

PHILIPS

B Ø 4 M PNX 8543 : AUDIO

B Ø 4 M

AUDIO-VDD
3H71 5K6
7H01-1 BC847BS(COL)
IH51
2H04 1u0
IH52
3H75 100R
FHV4
3H77 470R
2HYC 100p
AUDIO-VDD
7H01-2 BC847BS(COL)
3H74 5K6
IH53
2H05 1u0
IH55
3H76 100R
FHV5
IH54
3H94 470R
2HYD 100n
FH50
1HV9
1735446-3
2HVA 33p
3H18-1 22K
3H18-4 22K
2HVB 33p
+3V3
2HVC 100n
7HV0 TPA6111A2DGN
AMPLIFIER
VDD
IN-
VO
SHUTDOWN
BYPASS
VIA
GND_GND_HS
2H02 1u0
IH27
IHWJ
IHV1
AUDIO-HDPH-L-AP
AUDIO-HDPH-R-AP
ADAC(3)
ADAC(4)
IH47
IH48
2HVD 100n
2HVE 100n
IH24
IH25
3H18-3 22K
3H18-2 22K
IHWL
IHWE
2H25 3n3
2H26 3n3
RESET-AUDIO
3HV3 10K
+AUDIO-POWER
IH31
3H35 10K
3HV4-2 22K
IHW7
3HV4-1 22K
IHVA
BC847BPN(COL) 7HVA-2
A-PLOP
IH29
A-STBY
RESET-AUDIO
FHV3
3HV4-4 22K
IHW8
7HVA-1 BC847BPN(COL)
3HV4-3 22K
2HVG 1n0

1HV9 B3
2H02 D4
2H04 A2
2H05 B2
2H25 D1
2H26 D1
2HVA A5
2HVB B5
2HVC C5
2HVD C1
2HVE C2
2HVG E6
2HYC B3
2HYD C3
3H18-1 B5
3H18-2 C2
3H18-3 C2
3H18-4 B5
3H35 C7
3H71 A1
3H74 B1
3H75 A3
3H76 B2
3H77 B2
3H94 C2
3HV3 D2
3HV4-1 D7
3HV4-2 C8
3HV4-3 E6
3HV4-4 E6
7H01-1 A2
7H01-2 B2
7HV0 C4
7HVA-1 E7
7HVA-2 D8
FH50 B3
FHV3 E6
FHV4 A3
FHV5 C3
IH24 C2
IH25 C2
IH27 D4
IH29 D8
IH31 C8
IH47 C1
IH48 C1
IH51 A2
IH52 A2
IH53 B1
IH54 C2
IH55 B2
IHV1 C5
IHVA D8
IHW7 D7
IHW8 E7
IHWE C2
IHWJ C5
IHWL C2

CHN	SETNAME		
CLASS_NO	AUDIO	2	2008-11-21
	PNX8543 TV543 R2 LDIPNX	8204 000 8927	
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 16	130 – 13	A3
CHECK	DATE 2007-11-29	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

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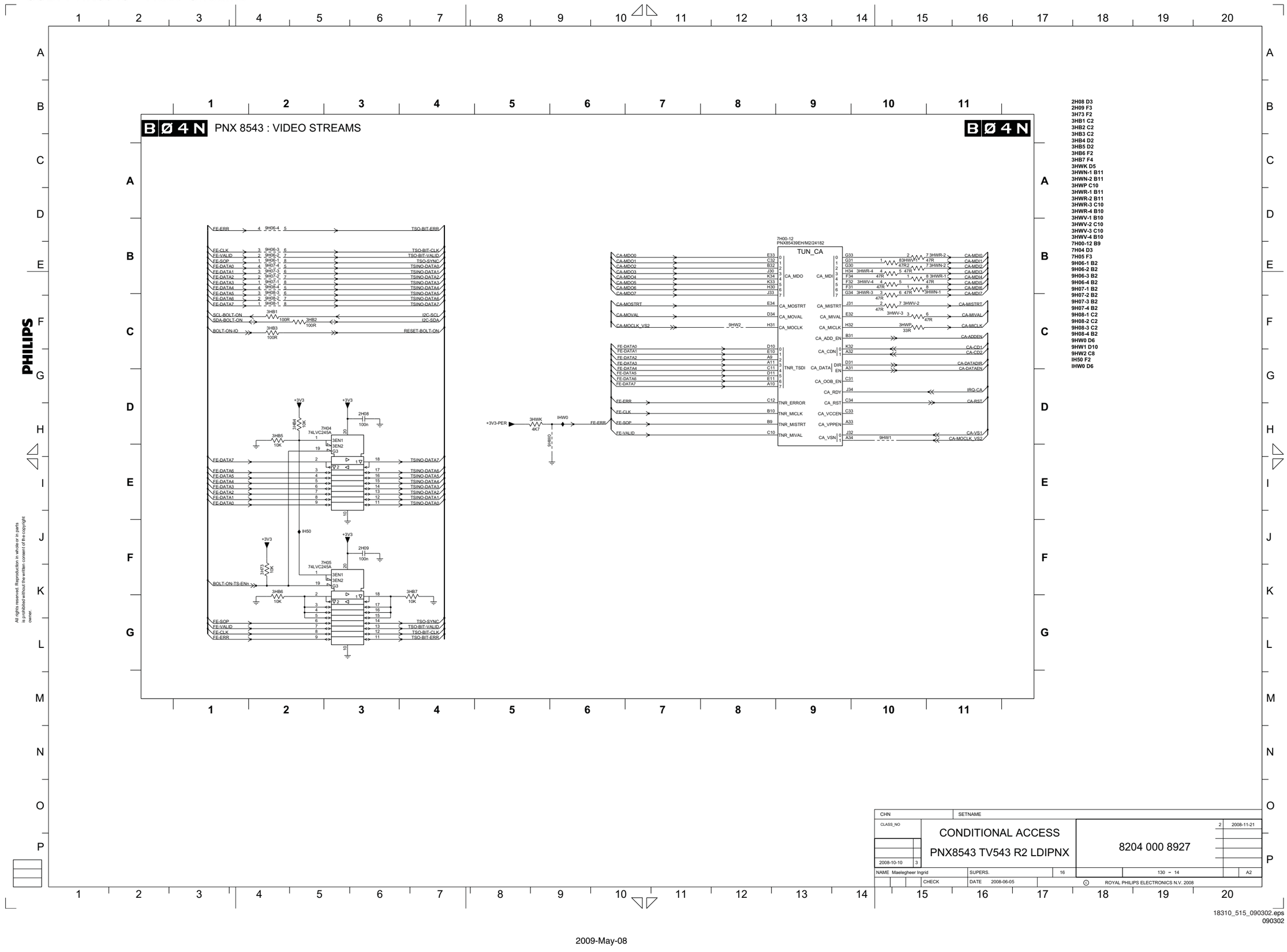
SSB: PNX8543 - Video Streams



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3HB2 C2
3HB3 C2
3HB4 D2
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3HB7 F4
3HWK D5
3HWN-1 B11
3HWN-2 B11
3HWP C10
3HWR-1 B11
3HWR-2 B11
3HWR-3 C10
3HWR-4 B10
3HWV-1 B10
3HWV-2 C10
3HWV-3 C10
3HWV-4 B10
7H00-12 B9
7H04 D3
7H05 F3
9H06-1 B2
9H06-2 B2
9H06-3 B2
9H06-4 B2
9H07-1 B2
9H07-2 B2
9H07-3 B2
9H07-4 B2
9H08-1 C2
9H08-2 C2
9H08-3 C2
9H08-4 B2
9HW0 D6
9HW1 D10
9HW2 C8
IH50 F2
IHW0 D6

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090302

SSB: PNX8543 - Digital Video Out/LVDS

B Ø 4 0 PNX8543 : DIGITAL VIDEO OUT / LVDS

3HP9 A7
7H00-11 B2
7H00-5 A6
IHPG A7

7H00-11
PNX85439EH/M2/24182

NC: W29, Y29, AA29, AB29, AC29, AD29, AE29, AF29, AG29, AH30, AJ30, AP30, AN31, AP31, AP32, M30, K31

Y4, R2, C4, R4, T4, W4, R5, W5, F11, F12, F13, F14, F15, C14, AJ11, AL12, AK15

AK28, AL28, AM28, AK29, AL29, AM29, AN29, K29, L29, M29, N29, P29, R29, T29, U29, V29

AL17, AN21, AP21, AL25, AM25, AN25, AP25, AK26, AL26, AM26, AN26, AP26, AM27, AN27

7H00-5
PNX85439EH/M2/24182

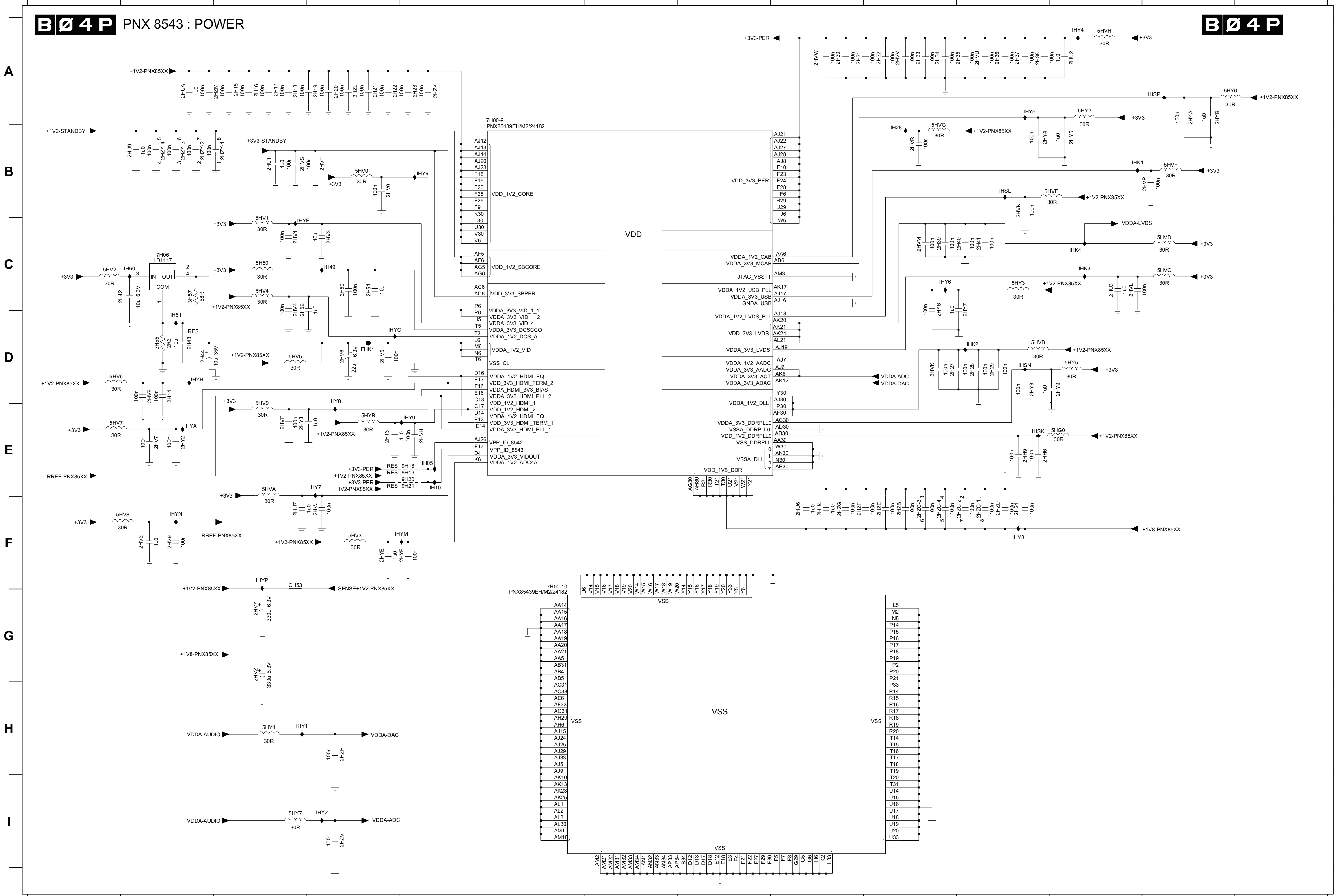
LVDS

IREF_LVDS	AK19	IHPG, 3HP9 12K 1%	VDDA-LVDS
A N	AN18		TX851A-
A P	AP18		TX851A+
B N	AK18		TX851B-
B P	AL18		TX851B+
C N	AN19		TX851C-
C P	AP19		TX851C+
D N	AN20		TX851D-
D P	AP20		TX851D+
E N	AL20		TX851E-
E P	AM20		TX851E+
CLK N	AL19		TX851CLK-
CLK P	AM19		TX851CLK+
LOUT2_A N	AN22		TX852A-
LOUT2_A P	AP22		TX852A+
LOUT2_B N	AK22		TX852B-
LOUT2_B P	AL22		TX852B+
LOUT2_C N	AN23		TX852C-
LOUT2_C P	AP23		TX852C+
LOUT2_D N	AN24		TX852D-
LOUT2_D P	AP24		TX852D+
LOUT2_E N	AL24		TX852E-
LOUT2_E P	AM24		TX852E+
LOUT2_CLK N	AL23		TX852CLK-
LOUT2_CLK P	AM23		TX852CLK+

CHN	SETNAME		
CLASS_NO	LVDS	2	2008-11-21
2008-10-10 3	PNX8543 TV543 R2 LDIPNX	8204 000 8927	
NAME Maelegheer Ingrid	SUPERS. 16	130 – 15	A3
CHECK	DATE 2007-11-29	ROYAL PHILIPS ELECTRONICS N.V. 2005	

18310_516_090302.eps
090302

SSB: PNX8543 - Power



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2H16 A3
2H17 A3
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2H20 A4
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2H22 A4
2H23 A5
2H24 F11
2H27 D10
2H28 D11
2H29 D11
2H30 A9
2H31 A9
2H32 A10
2H33 A10
2H34 A10
2H35 A10
2H36 A11
2H37 A11
2H38 A11
2H39 C10
2H40 C11
2H41 C11
2H42 C2
2H43 D2
2H44 D2
2H50 C4
2H51 C4
2H52 C3
2HH6 E11
2HH9 E11
2HU1 B3
2HU2 A12
2HU3 C12
2HU4 F9
2HU6 F9
2HU7 F3
2HU9 B2
2HUA A2
2HV0 B4
2HV1 C3
2HV2 F2
2HV3 C4
2HV4 C3
2HV5 D4
2HV6 D4
2HV7 E2
2HV8 D2
2HV9 F2
2HVF E3
2HVH E5
2HVJ F4
2HVK D10
2HVL C12
2HVM C10
2HVN B11
2HVP B13
2HVR B10
2HVS B3
2HVT B4
2HVU A11
2HVV A10
2HVW A9
2HVY G3
2HVZ G3
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2HY3 E3
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2HY7 C11
2HY8 D11
2HY9 D12
2HYA A13
2HYB A13
2HYE F4
2HYF F5
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2HZD F11
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2HZG F9
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2HZL A4
2HZM A3
2HZV I4
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2HZY-2 B2
2HZY-3 B2
2HZY-4 B2
3H55 D2
3H57 C2
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5HV6 D1
5HV7 E1
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5HVB D11
5HVC C13
5HVD C13
5HVE B12
5HVF B13
5HVG B10
5HVH A12
5HY2 A12
5HY3 C11
5HY4 H3
5HY5 D12
5HY6 A13
5HY7 I3
5HYB E4
7H00-10 F6
7H00-9 A6
7H06 C2
9H18 E5
9H19 E5
9H20 E5
9H21 E5
CH53 F3
FHK1 D4
IH05 E5
IH10 E5
IH28 B10
IH49 C4
IH60 C2
IH61 D2
IHK1 B12
IHK2 D11
IHK3 C12
IHK4 C12
IHSK E11
IHSL B11
IHSN D11
IHSP A13
IHY0 E5
IHY1 H3
IHY2 I4
IHY3 F11
IHY4 A12
IHY5 A11
IHY6 C10
IHY7 E4
IHY8 D4
IHY9 B5
IHYA E2
IHYC D4
IHYF C3
IHYH D2
IHYM F5
IHYN F2
IHYP F3

CHN | SETNAME | CLASS_NO
POWER
PNX8543 TV543 R2 LDIPNX
8204 000 8927
2 2008-11-21
2008-10-10 3
NAME Maelegheer Ingrid | SUPERS. 16 | 130 = 16 | A2
CHECK | DATE 2007-11-29

PHILIPS

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SSB: PNX5100 - SDRAM

B Ø 5 A PNX5100 : SDRAM

B Ø 5 A

PHILIPS

1C00 HOOK1

1X01 REF EMC HOLE

1C00 D9
2C00 E4
2C01 D4
2C02 E4
2C13 F4
2C14 F5
2C15 F5
2C16 F5
2C17 F5
2C18 F6
2C19 F6
2C29 E10
2C30 E10
2C32 F11
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2C35 F12
2C36 F12
2C38 F12
2C39 I12
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3C28-2 H11
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3C28-4 H12
3C30-1 H11
3C30-2 H11
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3C30-4 I9
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3C32 H12
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FC05 B11
FC06 B9
IC04 C2

CHN	SETNAME		
CLASS_NO	DDR2 PNX5100 TV543 R2 LDIPNX	8204 000 8928	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 9	130 – 1	A2
	CHECK DATE	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

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SSB: PNX5100 - Video-In

PHILIPS

BØSB

PNX5100 : VIDEO-IN

3C14 B2
3C15 B2
3C16 B2
3C17 C2
3C18 C2
3C19 D2
3C24 D2
3C29 D2
3C33 E2
3C34 E2
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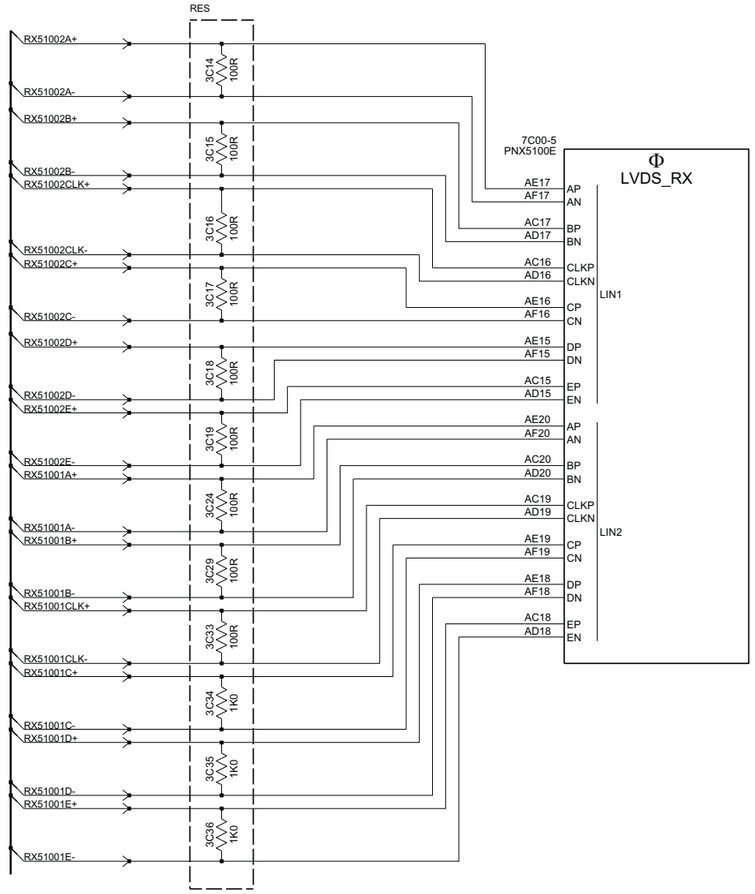
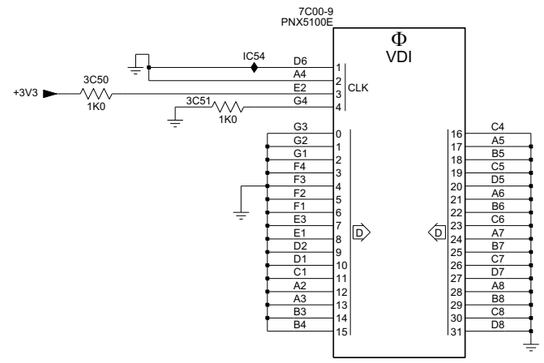
3C36 F2
3C50 C6
3C51 C7
7C00-5 B4
7C00-9 C7
IC54 C7





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CLASS_NO	VIDEO PNX5100	2	2008-11-21
	TV543 R2 LDIPNX	8204 000 8928	
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 9	130 – 2	A3
CHECK	DATE	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

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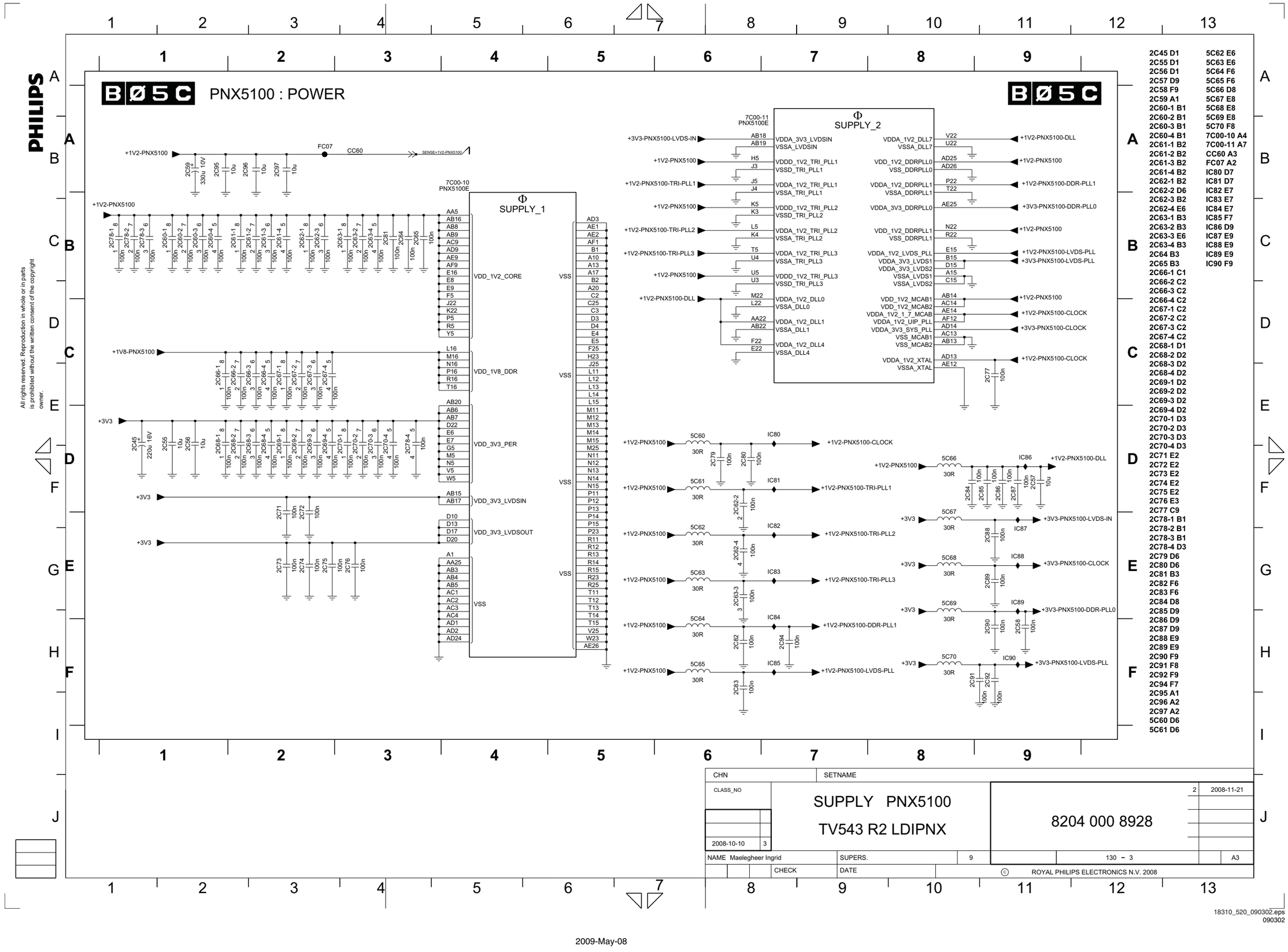
090302

SSB: PNX5100 - Power



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2C61-3 B2
2C61-4 B2
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2C86 D9
2C87 D9
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2C97 A2
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5C63 E6
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5C66 D8
5C67 E8
5C68 E8
5C69 E8
5C70 F8
7C00-10 A4
7C00-11 A7
CC60 A3
FC07 A2
IC80 D7
IC81 D7
IC82 E7
IC83 E7
IC84 E7
IC85 F7
IC86 D9
IC87 E9
IC88 E9
IC89 E9
IC90 F9

CHN	SETNAME		
CLASS_NO	SUPPLY PNX5100 TV543 R2 LDIPNX	2	2008-11-21
2008-10-10 3		8204 000 8928	
NAME Maelegheer Ingrid	SUPERS. 9	130 – 3	A3
CHECK	DATE	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_520_090302.eps
090302

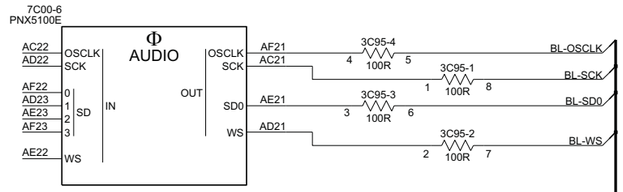
SSB: PNX5100 - Audio

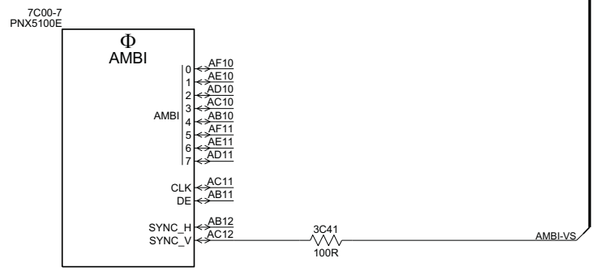
PHILIPS

B Ø 5 D PNX5100 : AUDIO

B Ø 5 D

3C41 D4
3C95-1 B5
3C95-2 B5
3C95-3 B4
3C95-4 B4
7C00-6 B3
7C00-7 C3

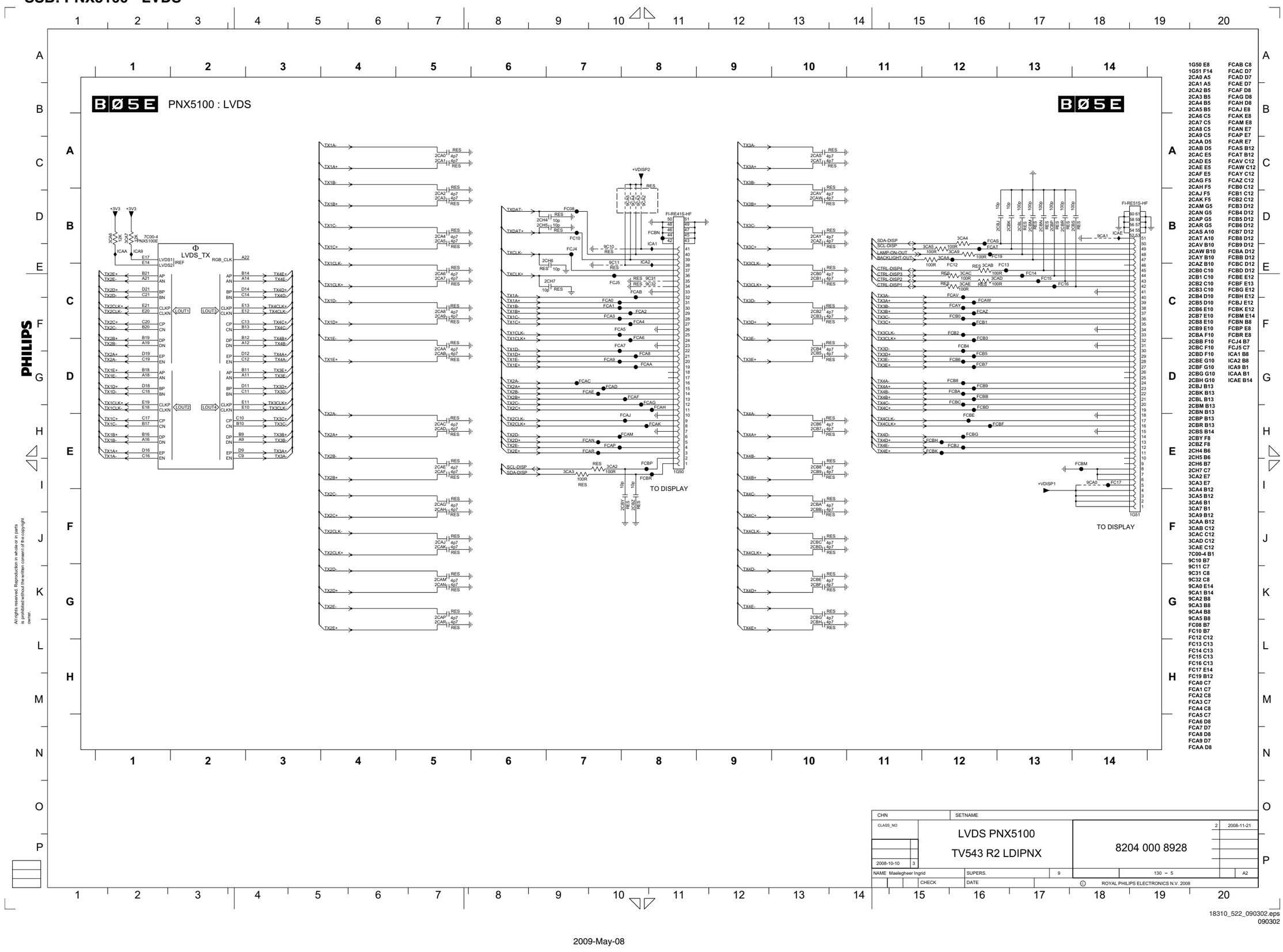




CHN	SETNAME		
CLASS_NO	AUDIO PNX5100 TV543 R2 LDIPNX	8204 000 8928	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 9	130 – 4	A3
CHECK	DATE	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

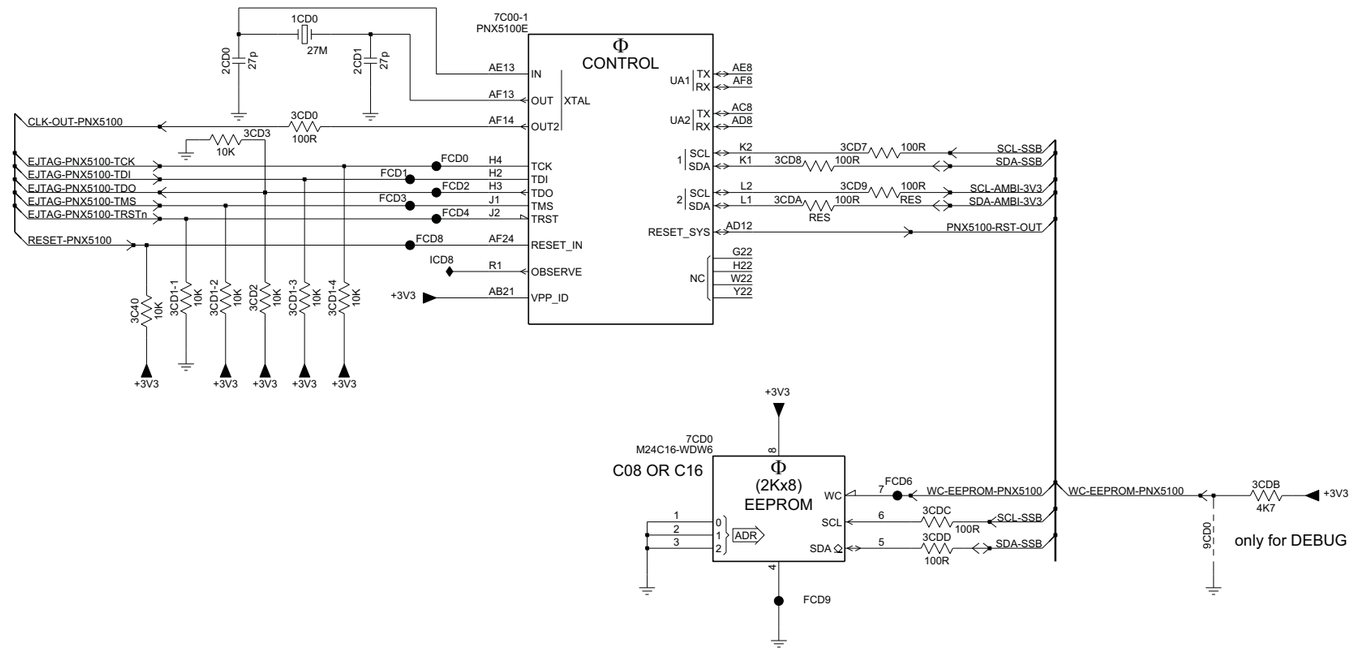
18310_521_090302.eps
090302

SSB: PNX5100 - LVDS



SSB: PNX5100 - Control

B Ø 5 F PNX5100 : CONTROL

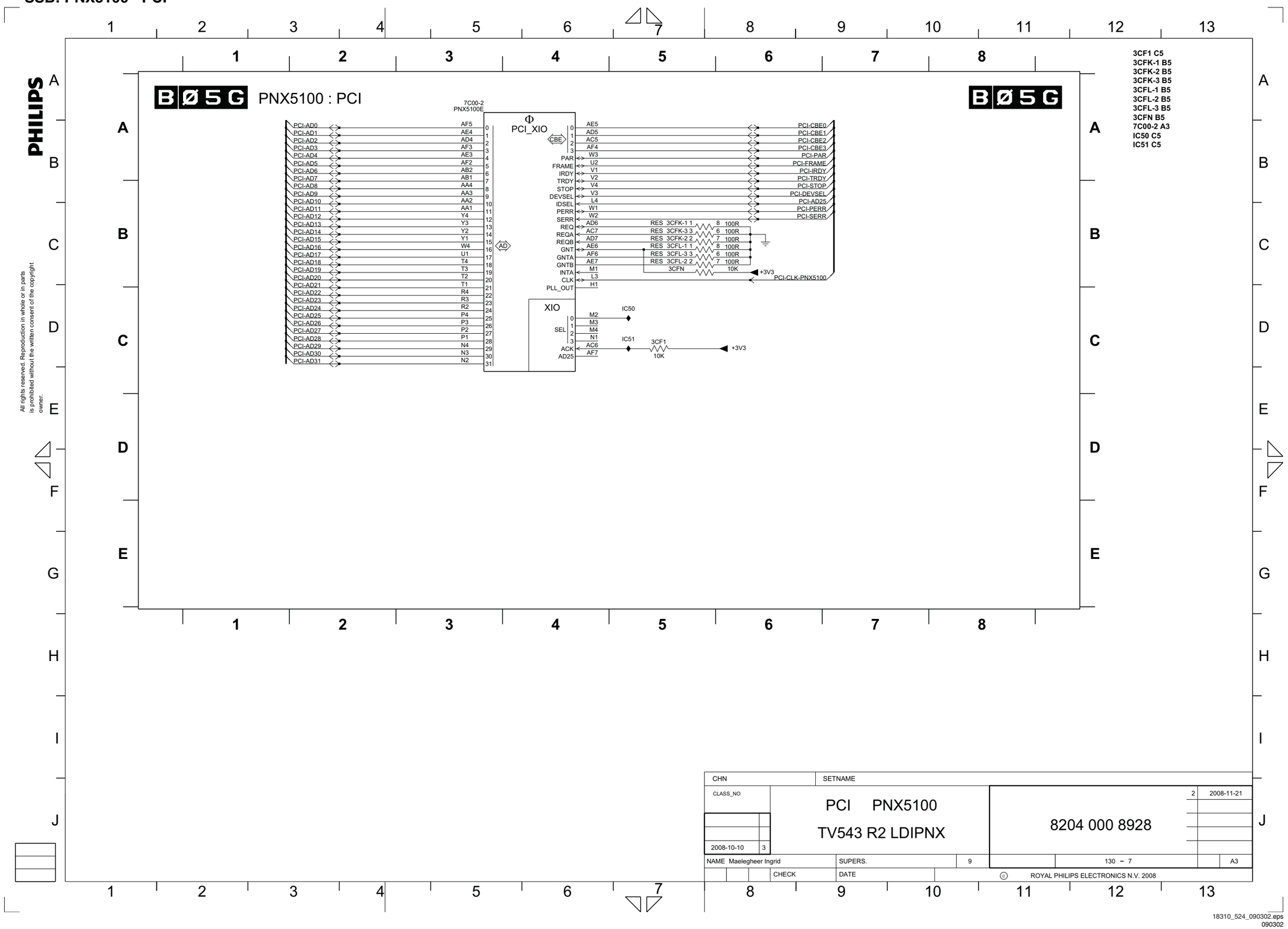


1CD0 A2
2CD0 A2
2CD1 A2
3C40 C1
3CD0 B2
3CD1-1 C2
3CD1-2 C2
3CD1-3 C2
3CD1-4 C1
3CD2 C2
3CD3 B2
3CD7 B5
3CD8 B5
3CD9 B5
3CDA B5
3CDB D7
3CDC D6
3CDD D6
7C00-1 A3
7CD0 C4
9CD0 D7
FCD0 B3
FCD1 B3
FCD2 B3
FCD3 B3
FCD4 B3
FCD6 D5
FCD8 B3
FCD9 D5
ICD8 B3

CHN	SETNAME		
CLASS_NO	CONTROL PNX5100 TV543 R2 LDIPNX	8204 000 8928	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 9	130 - 6	A3
CHECK	DATE	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

18310_523_090302.eps
090302

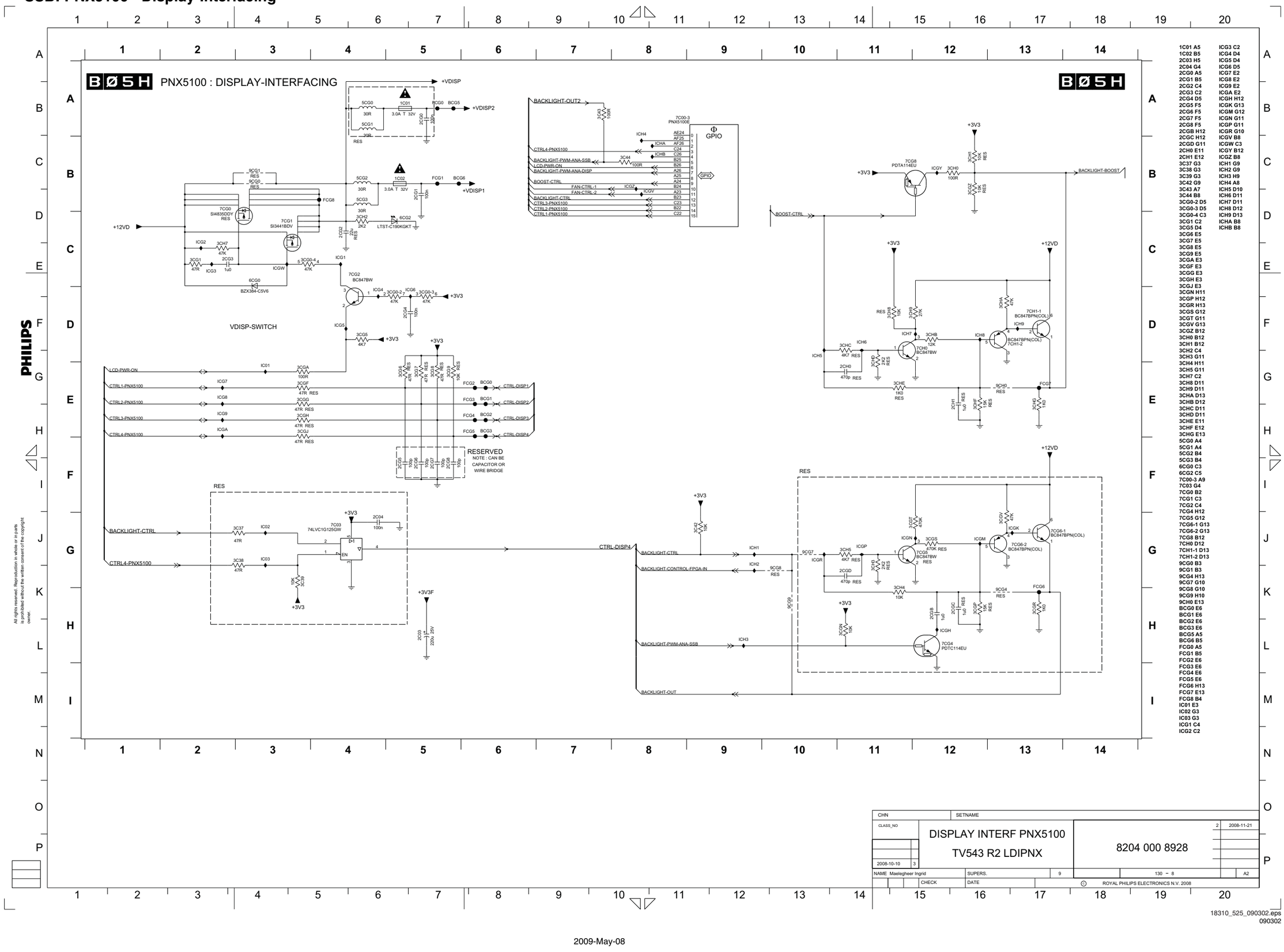
SSB: PNX5100 - PCI



CHN	SETNAME		
CLASS_NO	PCI PNX5100 TV543 R2 LDIPNX	8204 000 8928	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 9	130 – 7	A3
CHECK	DATE	ROYAL PHILIPS ELECTRONICS N.V. 2008	

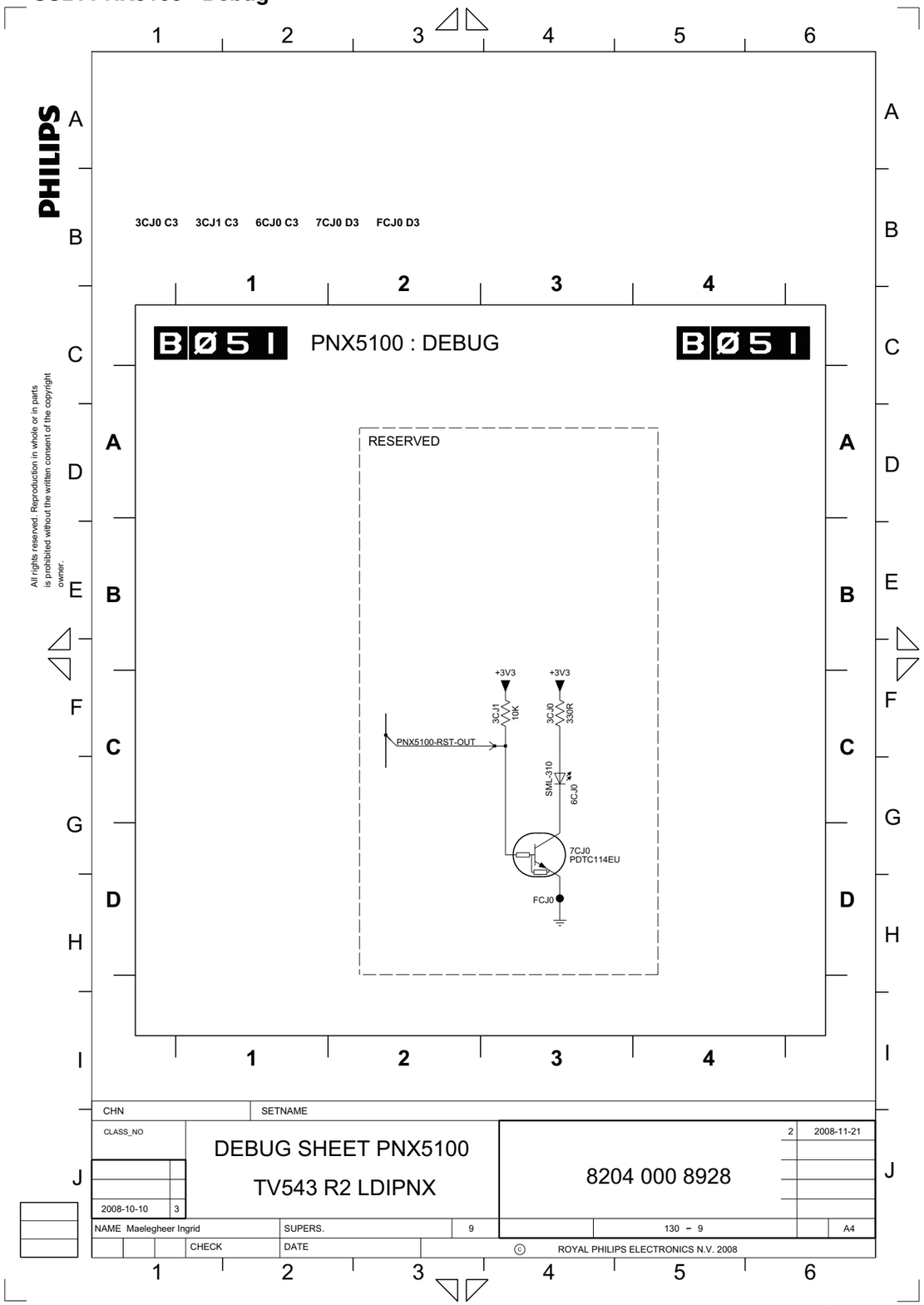
18310_524_090302.eps
090302

SSB: PNX5100 - Display-Interfacing



1C01 A5
1C02 B5
2C03 H5
2C04 G4
2CG0 A5
2CG1 B5
2CG2 C4
2CG3 C2
2CG4 D5
2CG5 F5
2CG6 F5
2CG7 F5
2CG8 F5
2CGB H12
2CGC H12
2CGD G11
2CH0 E11
2CH1 E12
3C37 G3
3C38 G3
3C39 G3
3C42 G9
3C43 A7
3C44 B8
3CG0-2 D5
3CG0-3 D5
3CG0-4 C3
3CG1 C2
3CG5 D4
3CG6 E5
3CG7 E5
3CG8 E5
3CG9 E5
3CGA E3
3CGF E3
3CGG E3
3CGH E3
3CGJ E3
3CGN H11
3CGP H12
3CGR H13
3CGS G12
3CGT G11
3CGV G13
3CGZ B12
3CH0 B12
3CH1 B12
3CH2 C4
3CH3 G11
3CH4 H11
3CH5 G11
3CH7 C2
3CH8 D11
3CH9 D11
3CHA D13
3CHB D12
3CHC D11
3CHD D11
3CHE E11
3CHF E12
3CHG E13
5CG0 A4
5CG1 A4
5CG2 B4
5CG3 B4
6CG0 C3
6CG2 C5
7C00-3 A9
7C03 G4
7CG0 B2
7CG1 C3
7CG2 C4
7CG4 H12
7CG5 G12
7CG6-1 G13
7CG6-2 G13
7CG8 B12
7CH0 D12
7CH1-1 D13
7CH1-2 D13
9CG0 B3
9CG1 B3
9CG4 H13
9CG7 G10
9CG8 G10
9CG9 H10
9CH0 E13
BCG0 E6
BCG1 E6
BCG2 E6
BCG3 E6
BCG5 A5
BCG6 B5
FCG0 A5
FCG1 B5
FCG2 E6
FCG3 E6
FCG4 E6
FCG5 E6
FCG6 H13
FCG7 E13
FCGB B4
IC01 E3
IC02 G3
IC03 G3
ICG1 C4
ICG2 C2
ICG3 C2
ICG4 D4
ICG5 D4
ICG6 D5
ICG7 E2
ICG8 E2
ICG9 E2
ICGA E2
ICGH H12
ICGK G13
ICGM G12
ICGN G11
ICGP G11
ICGR G10
ICGV B8
ICGW C3
ICGY B12
ICGZ B8
ICH1 G9
ICH2 G9
ICH3 H9
ICH4 A8
ICH5 D10
ICH6 D11
ICH7 D11
ICH8 D12
ICH9 D13
ICHA B8
ICHB B8

SSB: PNX5100 - Debug



18310_526_090302.eps
090302

Personal Notes:

10000_012_090121.eps
090121

SSB: FPGA Backlight-LVDS I²C-Mux

B Ø 6 A

FPGA Backlight-LVDS & I2C-MUX

RESERVED

FOR DEBUG

FOR FACTORY USE ONLY

TO AMBILIGHT

TO TEMPERATURE SENSOR

SPARTAN-3 FPGA

BANK0

BANK1

BANK2

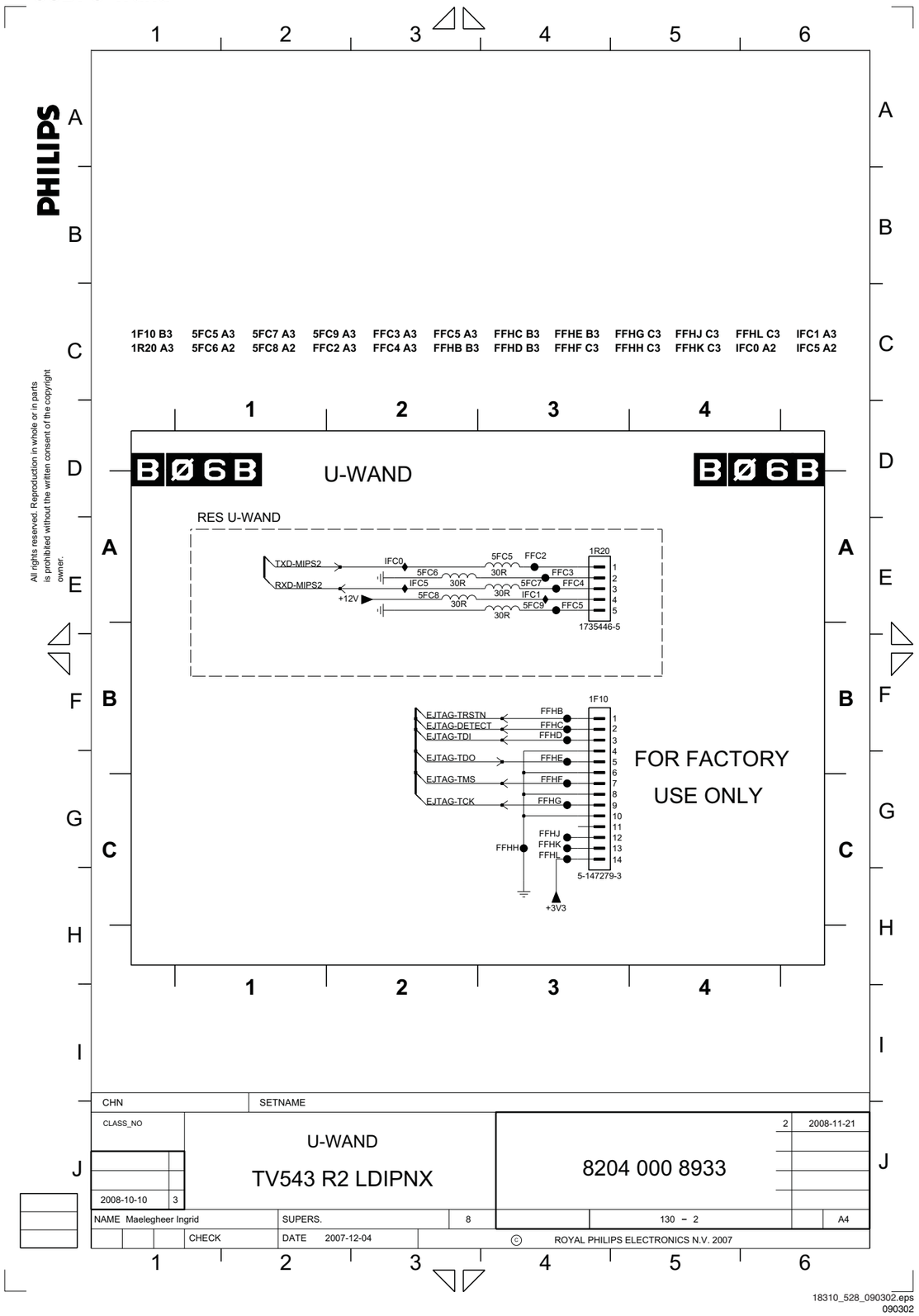
BANK3

1F03 H5	6F13 E2
1F05 H1	6F82 E6
1F29 I6	6F83 E6
1F50 B14	6F84 E6
1F53 E14	6F85 F6
1M59 A14	7F00 B8
1M71 C14	7F01 H9
2F00 I2	7F05 E2
2F01 H9	7F06 B2
2F02 I10	7F07 D2
2F03 D11	7F08 A6
2F04 C11	9F00 D11
2F05 I4	9F01 E11
2F06 D13	9F02 E11
2F07 D13	9F03 D10
2F08 E13	9F04 D7
2F09 C2	9F05-1 F9
2F10 C2	9F05-2 F9
2F11 D3	9F05-3 F9
2F12 C2	9F05-4 F9
2F13 C3	9F06 D10
2F14 C3	9F08 E10
2F15 C3	9F09 A5
2F16 C2	9F10 A5
2F17 C3	9F11 A5
2F18 D1	9F12 A5
2F19 D2	9F13 A8
2F20 B2	9F14 A8
2F21 C3	9F15 A8
2F22 B2	9F16 A8
2F23 B2	9F17 B6
2F24 B2	9F18 B6
2F25 B3	9F19 B6
2F26 A11	9F20 B6
2F27 A11	9FA1 A6
2F28 E13	9FA2 A6
2F29 F13	FF00 I2
2F30 A2	FF01 I1
2F31 A2	FF02 H10
2F32 A2	FF03 H8
2F33 A2	FF04 I8
2F34 B3	FF05 I8
2F35 B3	FF06 G4
2F36 A3	FF07 G4
2F37 A3	FF08 B6
2F38 A3	FF09 C3
2F39 A3	FF10 A3
2F40 F13	FF11 B6
2F41 G13	FF12 F7
2F42 G13	FF13 G5
2F46 C13	FF14 G4
2F47 C13	FF15 B6
2F48 C14	FF16 B6
2F49 A6	FF17 A3
2FA6 B13	FF20 B14
2FA7 B13	FF21 C14
2FND F11	FF22 C14
2FNE F11	FF23 F14
3F00-1 I3	FF24 F14
3F00-2 I2	FF25 F14
3F00-3 H2	FF30 G5
3F00-4 H2	FF31 F14
3F01 I2	FF40 E14
3F02 H8	FF41 E14
3F03 H10	FF42 E14
3F06 I8	FF43 E14
3F07 D11	FF44 E14
3F08 D11	FF54 F6
3F09 D11	FFA7 A13
3F10 E11	FFA8 A14
3F11 D7	FFA9 A13
3F12 C11	IF00 H9
3F13 C10	IF01 F10
3F14 F7	IF02 D10
3F15-1 G4	IF07 C10
3F15-2 G4	IF08 D9
3F15-3 G5	IF09 C10
3F16-1 H4	IF12 B3
3F16-2 H4	IF13 C10
3F16-3 H4	IF14 D7
3F16-4 H5	IF15 D10
3F17 D13	IF16 D10
3F18 D13	IF17 D10
3F19 E13	IF18 D9
3F20 E13	IF19 E9
3F21 F13	IF20 C13
3F22 E7	IF21 C13
3F23 E7	IF29 B14
3F24 E1	IF32 E7
3F25 E2	IF33 E7
3F26 F6	IF34 F7
3F27 F2	IF35 F7
3F28 F4	IF36 E10
3F29 F13	IF37 E10
3F30 G13	IF38 F10
3F31 G13	IF39 F10
3F36 A8	IFA8 A11
3F37 A8	IFA9 A10
3F38 A8	
3F39 B8	
3F40 C13	
3F41 C13	
3F79 F10	
3F80 F10	
3F82 E7	
3F83 E7	
3F84 E7	
3F85 E7	
3FA5 A12	
3FA6 A12	
3FAA A10	
3FAB A10	
5F02 C1	
5F03 A2	
5F04 A2	
5F05 B14	
5F06 B14	

CHN	SETNAME		
CLASS_NO	FPGA Backlight-LVDS & I2C-MUX TV543 R2 LDIPNX	8204 000 8933	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 8	130 ~ 1	A2
CHECK	DATE 2007-12-04	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

18310_527_090302.eps
090302

SSB: U-Wand



18310_528_090302.eps
090302

Personal Notes:

10000_012_090121.eps
090121

SSB: Temperature & Fan control

B Ø 6 C TEMPERATURE- & FAN-CONTROL

B Ø 6 C

1F01 FF49 +12V FF50 FAN1-DRV
FF51 TACHO1
2F50 1u0 2F51 100p 2F52 1u0

1F02 +12V FF52 FAN2-DRV
FF53 TACHO2
2F53 1u0 2F54 100p 2F55 1u0

+12V 1K0 3F59 SML-310 6F51 IF50
FAN1-DRV 3F51 10R 7F52 BCP53 IF51 3F53 100R IF52
FAN2-DRV 3F56 10R
RES 3F57 10R IF55 RES 7F55 BCP53 IF56 RES 3F58 100R

+12V 3F50 10K 7F53 BC857BW IF67 3F54 100R IF53 3F55 22K IF54
2F56 RES 2F57 1u0 10u

+12V 3F52 10K +3V3 PDTC114EU 7F57 RES 3F70 10K IF59
9F07 RES
FAN1-OUT
FAN-CTRL-1

+3V3 3F60 1K0 6F50 SML-310 2F58 100n
7F50 LM75ADP
SDA-SET 3F61 100R IF63 IF65
SCL-SET 3F62 100R
OS +VS A0 A1 A2 SDA SCL GND
IF62 IF64 IF66
9F50 9F51 3F65 RES 1K0
3F63 RES 1K0 3F64 RES 1K0 9F52

+3V3 2F59 100n
7F51 VDD LED0 LED1 LED2 LED3 PCA9533 VSS
SCL-SET 3F66 100R IF69 SCL
SDA-SET 3F67 100R IF68 SDA
FAN1-OUT
TACHO1-INV
TACHO2-INV

+12V 7F54 PDTA114EU TACHO1
TACHO1-INV IF58 3F68 27K IF57 2F60 100n 3F69 10K

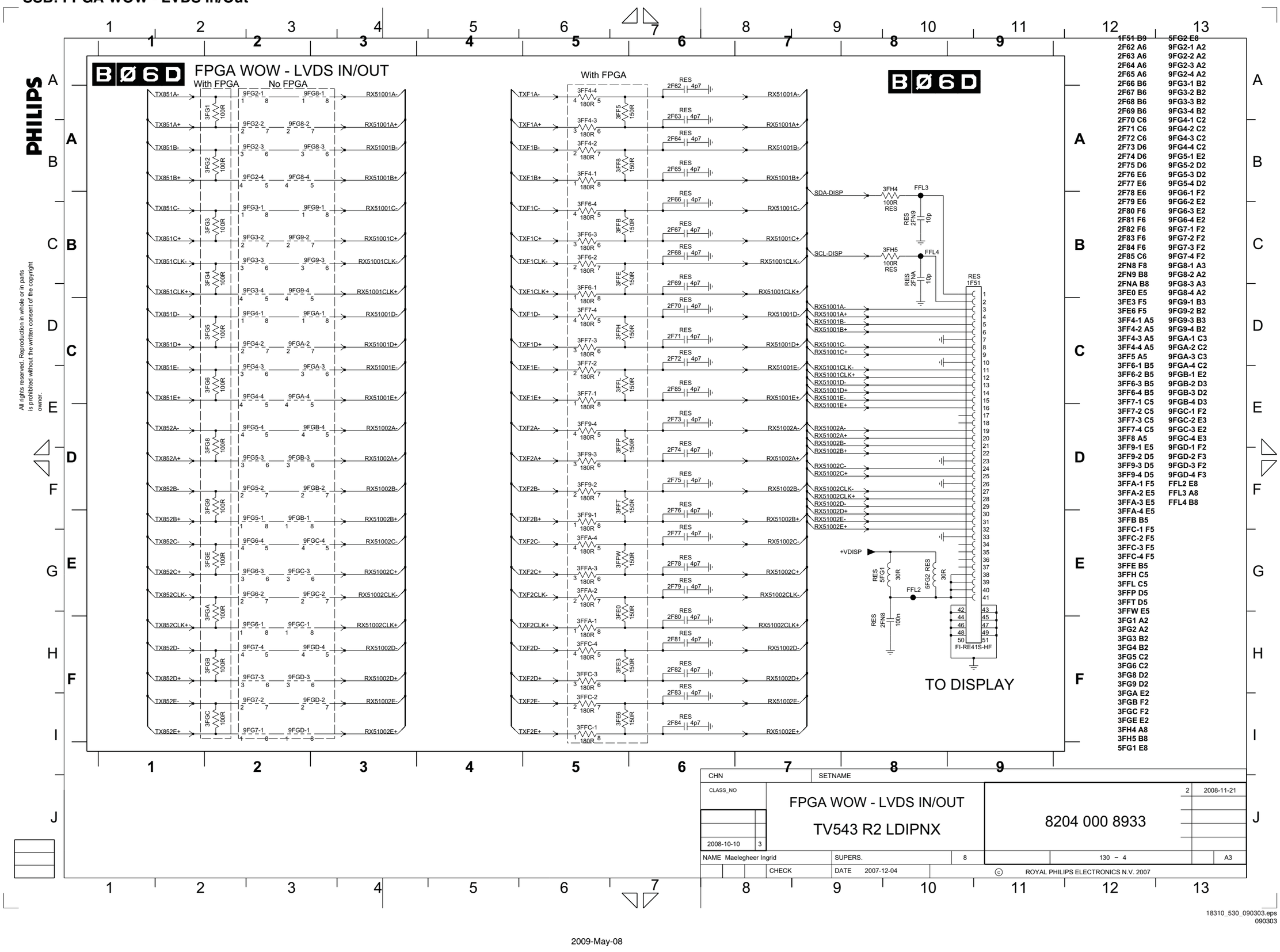
+3V3 RES 3F73 1K0 +12V 7F56 PDTA114EU TACHO2
TACHO2-INV IF61 3F71 27K IF60 2F61 100n 3F72 10K

1F01 A1 IF66 B9
1F02 B1 IF67 E4
2F50 B2 IF68 D7
2F51 B2 IF69 D7
2F52 B2
2F53 C2
2F54 C2
2F55 C2
2F56 E4
2F57 E4
2F58 B8
2F59 C8
2F60 E8
2F61 F8
3F50 E3
3F51 E2
3F52 E5
3F53 E3
3F54 E4
3F55 E5
3F56 E2
3F57 F2
3F58 F3
3F59 D2
3F60 A7
3F61 B7
3F62 B7
3F63 C8
3F64 C9
3F65 B9
3F66 D7
3F67 D7
3F68 E8
3F69 E8
3F70 E6
3F71 F8
3F72 F8
3F73 F8
6F50 B7
6F51 D2
7F50 B7
7F51 C8
7F52 D3
7F53 E4
7F54 D9
7F55 E3
7F56 F9
7F57 F6
9F07 F6
9F50 B8
9F51 B9
9F52 C9
FF49 A2
FF50 A3
FF51 B3
FF52 C3
FF53 C3
IF50 D2
IF51 E3
IF52 E3
IF53 E4
IF54 E5
IF55 F2
IF56 F3
IF57 E8
IF58 E8
IF59 E6
IF60 F8
IF61 F8
IF62 B8
IF63 B7
IF64 B9
IF65 B7

CHN	SETNAME		
CLASS_NO	TEMPERATURE- & FAN-CONTROL	2	2008-11-21
	TV543 R2 LDIPNX	8204 000 8933	
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 8	130 – 3	A3
	CHECK DATE 2007-12-04	© ROYAL PHILIPS ELECTRONICS N.V. 2007	

18310_529_090303.eps
090303

SSB: FPGA WOW - LVDS In/Out



SSB: FPGA WOW - Power & Control

B Ø 6 E FPGA WOW - POWER & CONTROL

B Ø 6 E

PHILIPS

FFH0 → +1V2-PLL

+1V2-PNX85XX → CFH0 → FFH1 → +1V2-FPGA

+3V3 → 5FH1 30R → FFH2 → +3V3-FPGA

+2V5 → 5FH2 30R → FFH3 → +2V5out-FPGA

+2V5 → 5FH3 30R → FFH4 → +2V5in-FPGA

+2V5 → 5FH4 30R → FFHA → +2V5-PLL

+1V8-PNX85XX → CFH1 → +1V8-PNX5100

FOR DEBUG

CON27 CON26 CON23 CON22 CON21 CON20

3FH0 3FH1 3FH2 3FH3 3FH8 3FH7 470R

6FH0 6FH1 6FH2 6FH3 6FH8 6FH7 LTST-C150KGKT

IFH4 +3V3

7FH0 M25P16 16M FLASH

FFHP ASDO FFHN DCLK FFHM nCSO FFHR DATA0 FFHS

3FHG 47R

+2V5in-FPGA +3V3

3FHM 1M0 3FHL 10K 6FH8 SML-310

CONF-DONE FFHT 3FHK 100K 3FHJ 100K 7FH2 BC847BW

+2V5 +2V5 +2V5

3FH9-3 1M0 3FH9-2 1M0 3FH9-1 1M0 9FH0 RES 2FJ7 RES 10n

TCK TDO TMS TDI

3FHB-1 3FHB-4 3FHB-2 3FHB-3 100R

FFH5 FFH6 FFH7 FFH8 FFH9

1F00 5-1472279-2

FOR DEBUG

2FJ3 2FJ4 2FJ5 2FJ6 2FJ1 2FJD RES 100p RES 1n

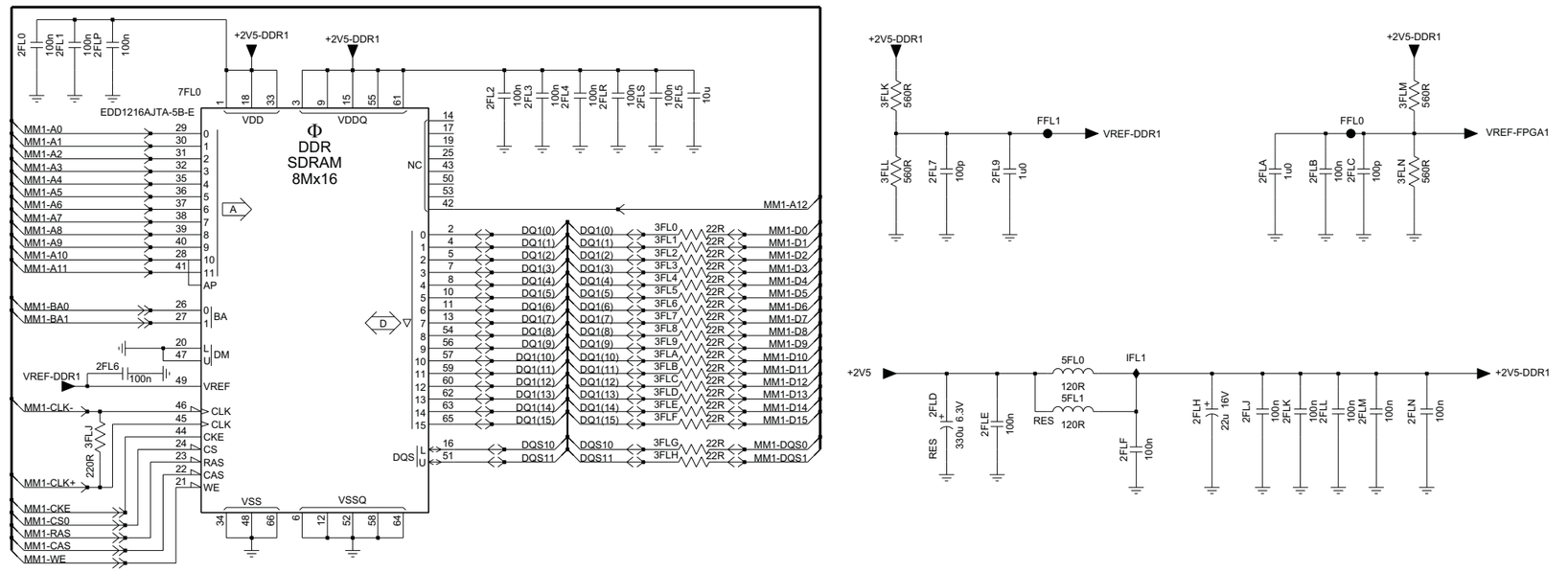
1F00 E12
2FH0 B5
2FH1 B5
2FH2 A3
2FH3 A3
2FH4 A3
2FH5 A4
2FH6 E2
2FH7 E2
2FH8 E3
2FH9 E3
2FHA A3
2FHB C3
2FHC B3
2FHD B4
2FHE B4
2FHF B4
2FHG B4
2FHH B4
2FHJ B5
2FHK B5
2FHL B2
2FHM B2
2FHN C2
2FHP C3
2FHR C3
2FHS C3
2FHT B3
2FHV C3
2FHW D3
2FHZ D3
2FJ0 D3
2FJ1 D2
2FJ2 D2
2FJ3 F11
2FJ4 F11
2FJ5 F11
2FJ6 F11
2FJ7 D12
2FJ8 C2
2FJ9 C2
2FJA C3
2FJB C3
2FJC C3
2FJD F12
2FJJ B8
2FJK B7
2FJP B3
3FH0 H2
3FH1 H2
3FH2 H2
3FH3 H3
3FH6 H3
3FH7 H3
3FH8 D9
3FH9-1 D9
3FH9-2 D9
3FH9-3 E9
3FHB-1 E10
3FHB-2 E10
3FHB-3 E10
3FHB-4 E10
3FHG C9
3FHJ C12
3FHK C12
3FHL B11
3FHM B12
5FH0 A2
5FH1 B2
5FH2 C2
5FH3 D2
5FH4 E2
6FH0 I2
6FH1 I2
6FH2 I2
6FH3 I3
6FH6 I3
6FH7 I3
6FH8 B12
7FH0 B8
7FH2 C12
9FH0 D11
CFH0 B2
CFH1 D6
FFH0 A3
FFH1 B3
FFH2 B3
FFH3 C3
FFH4 D3
FFH5 E10
FFH6 E10
FFH7 E10
FFH8 E10
FFH9 E10
FFHA E3
FFHM B9
FFHN B9
FFHP B9
FFHR C9
FFHS C9
FFHT C11
IFH4 A7

CHN	SETNAME		
CLASS_NO	FPGA WOW - POWER & CONTROL	2	2008-11-21
	TV543 R2 LDIPNX	8204 000 8933	
2008-10-10	3		
NAME Maelegheer Ingrid	SUPERS.	8	130 - 5 A2
	CHECK	DATE 2007-12-04	

18310_531_090303.eps
090303

SSB: FPGA WOW - DDR

BØ6F FPGA WOW - DDR

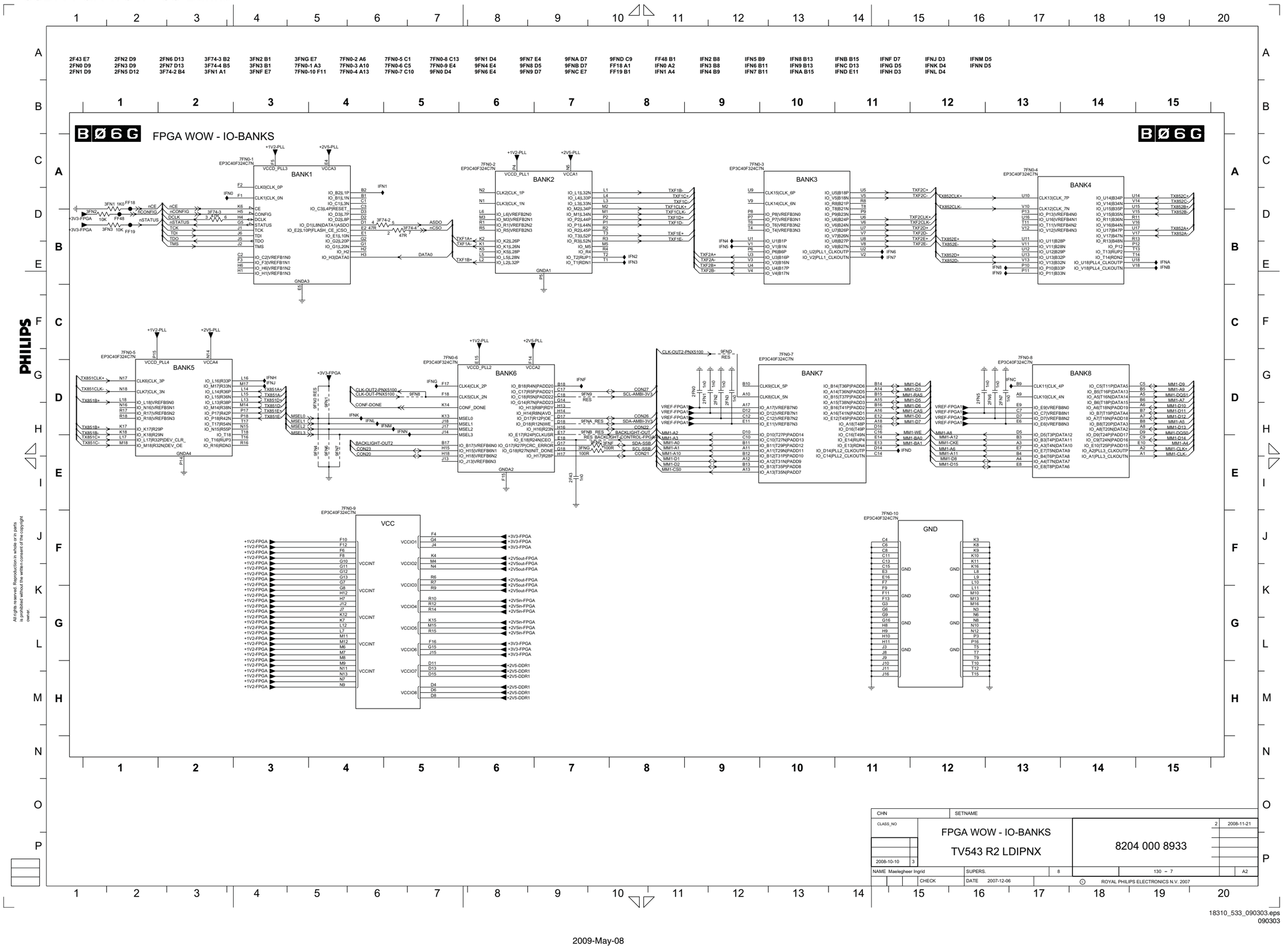


2FL0 A1
2FL1 A1
2FL2 B3
2FL3 B4
2FL4 B4
2FL5 B5
2FL6 C1
2FL7 B6
2FL9 B6
2FLA B8
2FLB B8
2FLC B8
2FLD C6
2FLE C6
2FLF D7
2FLH C7
2FLJ C8
2FLK C8
2FLL C8
2FLM C8
2FLN C9
2FLP A1
2FLR B4
2FLS B4
3FL0 B4
3FL1 B4
3FL2 C4
3FL3 C4
3FL4 C4
3FL5 C4
3FL6 C4
3FL7 C4
3FL8 C4
3FL9 C4
3FLA C4
3FLB C4
3FLC C4
3FLD C4
3FLE C4
3FLF C4
3FLG D4
3FLH D4
3FLJ D1
3FLK B6
3FLL B6
3FLM B9
3FLN B9
5FL0 C7
5FL1 C7
7FL0 B2
FFL0 B8
FFL1 B7
IFL1 C7

CHN	SETNAME		
CLASS_NO	FPGA WOW - DDR TV543 R2 LDIPNX	8204 000 8933	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 8		
CHECK	DATE 2007-12-04	130 – 6	A3

18310_532_090303.eps
090303

SSB: FPGA WOW - I/O Banks



SSB: CI: PCMCIA Connector

1P00-A B1 1P00-B B5 2P15 A8 | 2P16 C8 2P40 A2 3P09 A2 | 3P10-1 A6 3P10-2 A6 3P10-4 A6 | 3P11 C7 3P12 A6 3P13-1 A6 | 3P13-2 A6 3P13-3 A6 3P20 D2 | 3P24 D6 3P25 E6 3P26-1 E6 | 3P26-2 E6 3P26-3 E6 3P26-4 E6 | 3P27-1 E6 3P27-2 E6 3P27-3 E6 | 3P27-4 E6 3P80-1 B9 3P80-2 B9 | 3P80-3 B9 3P80-4 B9 3P81 B9 | 3P82-1 D9 3P82-2 D9 3P82-3 D9 | 3P82-4 D9 3P83-3 D9 3P83-4 D9 | 3P84-1 E8 3P84-2 E8 3P84-3 E8 | 3P84-4 E8 3P85-1 E8 3P85-2 E8 | 3P85-3 E8 3P85-4 E8 3P86 E8 | 3P87 E8 3P88 E8 7P15 A8 | 7P16 C8 FP04 A2 FP05 D6 | IP00 A6 IP01 A6 IP02 A6 | IP03 A6 IP04 A6 IP05 A6 | IP08 D2 IP09 C9 IP18 D2

B Ø 7 A CI : PCMCIA CONNECTOR **B Ø 7 A**

CABLE CARD INTERFACE

+5V — 3P09 0R4 (+T) — FP04 — PCMCIA-VCC-VPP; 2P40 22u

ROW_A 1P00-A

1	GND1	
2	D3	PCMCIA-D3
3	D4	PCMCIA-D4
4	D5	PCMCIA-D5
5	D6	PCMCIA-D6
6	D7	PCMCIA-D7
7	CE1	CA-CE1
8	A10	PCMCIA-A10
9	OE	CA-OE
10	A11	PCMCIA-A11
11	A9	PCMCIA-A9
12	A8	PCMCIA-A8
13	A13	PCMCIA-A13
14	A14	PCMCIA-A14
15	WE|P	CA-WE
16	RDY|BSY	IRQ-CA
17	VCC1	PCMCIA-VCC-VPP
18	VPP1	
19	A16	CA-MIVAL
20	A15	CA-MICLK
21	A12	PCMCIA-A12
22	A7	PCMCIA-A7
23	A6	PCMCIA-A6
24	A5	PCMCIA-A5
25	A4	PCMCIA-A4
26	A3	PCMCIA-A3
27	A2	PCMCIA-A2
28	A1	PCMCIA-A1
29	A0	PCMCIA-A0
30	D0	PCMCIA-D0
31	D1	PCMCIA-D1
32	D2	PCMCIA-D2
33	WP|IOIS16	
34	GND2	

WP|IOIS16 — 3P20 10K — IP08 — PCMCIA-VCC-VPP; GND2 — IP18; 69 70

+3V3 PCMCIA-VCC-VPP

3P10-4 10K — IP00 — CA-INPACK
3P10-2 10K — IP01 — CA-WAIT
3P10-1 10K — MOCLK_VS2
RES 3P12 10K — IP02 — IRQ-CA
3P13-1 10K — IP03 — CA-CD1
3P13-3 10K — IP04 — CA-CD2
3P13-2 10K — IP05 — CA-VS1

ROW_B 1P00-B

35	GND3	
36	CD1	CA-CD1
37	D11	MDO3
38	D12	MDO4
39	D13	MDO5
40	D14	MDO6
41	D15	MDO7
42	CE2	CA-CE2
43	VS1	CA-VS1
44	IORD	CA-IORD
45	IOWR	CA-IOWR
46	A17	CA-MISTRT
47	A18	CA-MDI0
48	A19	CA-MDI1
49	A20	CA-MDI2
50	A21	CA-MDI3
51	VCC2	PCMCIA-VCC-VPP
52	VPP2	
53	A22	CA-MDI4
54	A23	CA-MDI5
55	A24	CA-MDI6
56	A25	CA-MDI7
57	VS2	MOCLK_VS2
58	RESET	CA-RST
59	WAIT	CA-WAIT
60	INPACK	CA-INPACK
61	REG	CA-REG
62	BVD2|SPKR	MOVAL
63	BVD1|STSCHG	MOSTRT
64	D8	MDO0
65	D9	MDO1
66	D10	MDO2
67	CD2	CA-CD2
68	GND4	

71 72 — FP05

3P24 10K — MOSTRT
3P25 10K — MOVAL
3P26-3 10K — MDO0
3P26-2 10K — MDO1
3P26-1 10K — MDO2
3P26-4 10K — MDO3
3P27-4 10K — MDO4
3P27-3 10K — MDO5
3P27-2 10K — MDO6
3P27-1 10K — MDO7

+3V3 — 2P15 100n — 7P15 74LVC245A (20; 3EN1 1; 3EN2 19; G3; 10)

MDO3 18 — 3P80-4 47R — CA-MDO3
MDO4 17 — 3P80-3 47R — CA-MDO4
MDO6 16 — 3P80-2 47R — CA-MDO6
MDO5 15 — 3P80-1 47R — CA-MDO5
MDO7 14 — 3P81 47R — CA-MDO7
13
12
11

+3V3 — 2P16 100n — 7P16 74LVC245A (20; 3EN1 1; 3EN2 19; G3; 10)

CA-RST — 3P11 100K
MOCLK_VS2 18 — 3P82-4 47R — IP09 — CA-MOCLK_VS2
MDO0 17 — 3P82-3 47R — CA-MDO0
MDO2 16 — 3P82-2 47R — CA-MDO2
MDO1 15 — 3P82-1 47R — CA-MDO1
MOVAL 14 — 3P83-4 47R — CA-MOVAL
MOSTRT 13 — 3P83-3 47R — CA-MOSTRT
12
11

RESERVED

MDO3 — 3P84-4 47R — CA-MDO3
MDO4 — 3P84-3 47R — CA-MDO4
MDO5 — 3P84-1 47R — CA-MDO5
MDO6 — 3P84-2 47R — CA-MDO6
MDO7 — 3P88 47R — CA-MDO7
MDO1 — 3P85-2 47R — CA-MDO1
MDO2 — 3P85-3 47R — CA-MDO2
MDO0 — 3P85-4 47R — CA-MDO0
MOVAL — 3P85-1 47R — CA-MOVAL
MOSTRT — 3P86 47R — CA-MOSTRT
MOCLK_VS2 — 3P87 47R — CA-MOCLK_VS2

1X06 EMC HOLE

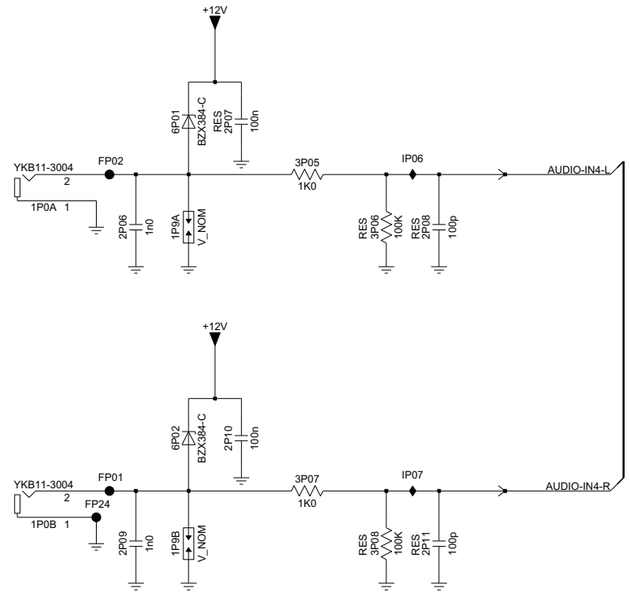
1X05 REF EMC HOLE

CHN	SETNAME		
CLASS_NO	UFD2K8 DIGI i/O TV543 R2 LDIPNX	2	2008-11-21
2008-10-10 3		8204 000 8934	
NAME Maelegheer Ingrid	SUPERS. 8	130 – 1	A3
CHECK	DATE 2007-10-18	© ROYAL PHILIPS ELECTRONICS N.V. 2007	

18310_534_090303.eps
090303

SSB: Audio In HDMI

B Ø 7 B AUDIO IN HDMI



1P0A B2
1P0B D2
1P9A B3
1P9B D3
2P06 B2
2P07 B3
2P08 B4
2P09 D2
2P10 D3
2P11 D4
3P05 B3
3P06 B4
3P07 D3
3P08 D4
6P01 B3
6P02 D3
FP01 D2
FP02 B2
FP24 D2
IP06 B4
IP07 D4

CHN	SETNAME		
CLASS_NO	UFD2K8	2	2008-11-21
2008-10-10 3	DIGI I/O TV543 R2 LDIPNX	8204 000 8934	
NAME Maelegheer Ingrid	SUPERS. 8	130 – 2	A3
CHECK	DATE 2007-10-18	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

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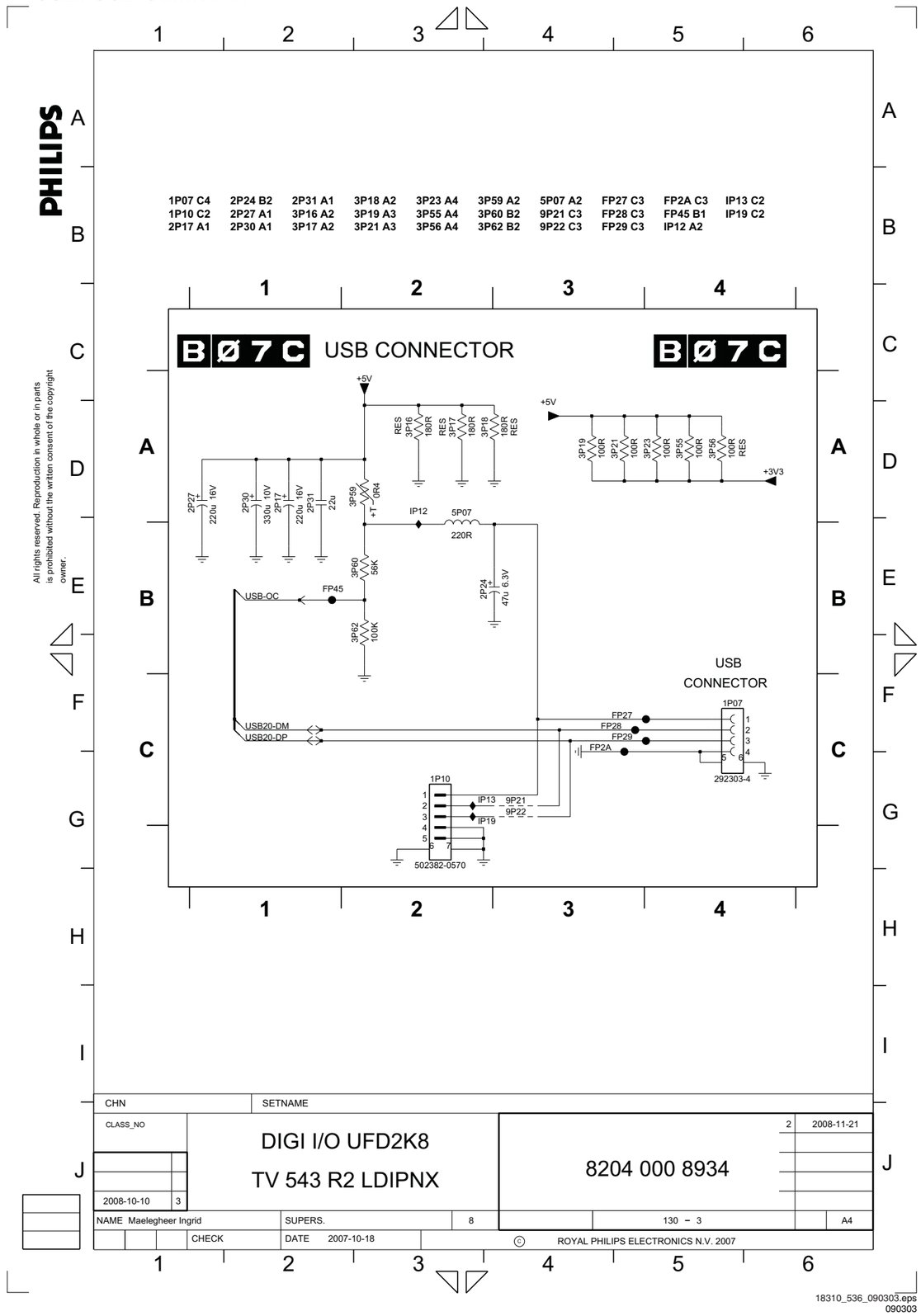
090303

SSB: USB Connector



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090303

Personal Notes:

10000_012_090121.eps
090121

SSB: HDMI

B Ø 7 D HDMI

HDMI CONNECTOR 3

HDMI CONNECTOR 2

HDMI CONNECTOR 1

HDMI CONNECTOR SIDE

RES

Remark for service:

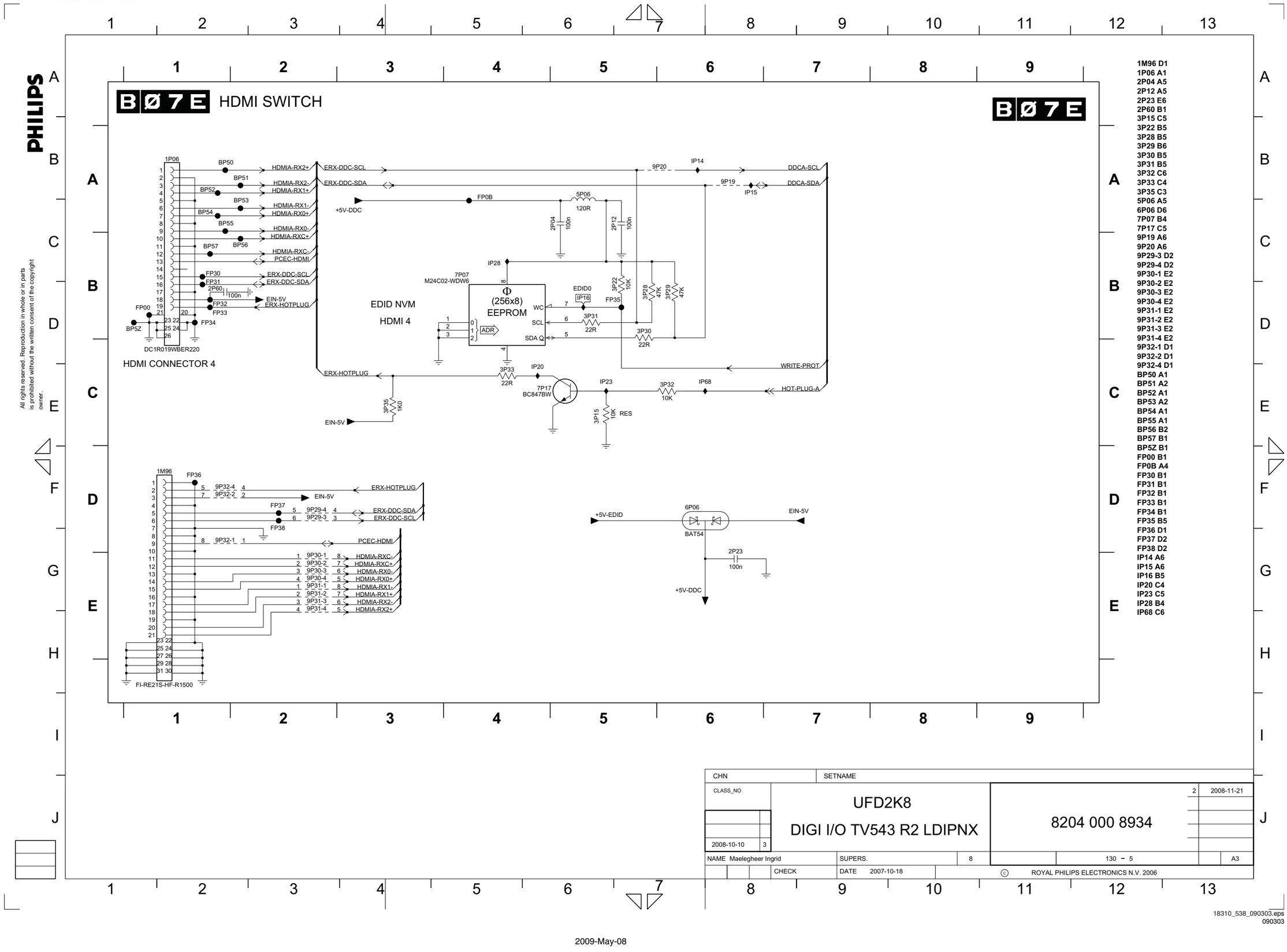
I2C Address = 0xCE
Replacing the TDA 9996
Requires reprogramming
of its I2C address from
0xC0 to 0xCE

1P02 E1 FP0S I1
1P03 C1 FP0T I2
1P04 A1 FP0U I2
1P05 H1 FP0W I1
2P03 C6 FP10 B1
2P05 C10 FP11 B1
2P28 H13 FP12 B1
2P32 H13 FP13 B1
2P33 I12 FP14 B2
2P34 D12 FP15 B1
2P35 D12 FP16 G1
2P36 D10 FP17 I1
2P37 D10 FP20 B11
2P38 D9 FP21 E9
2P39 D9 FP22 H12
2P41 D9 FP23 I10
2P42 D9 FP25 D8
2P43 D12 FP26 D12
2P44 C10 FP39 C12
2P45 C11 FP40 C11
2P46 B10 FP41 C10
2P47 C10 FP42 A6
2P48 A5 FP43 H12
2P49 A6 FP44 F13
2P50 D12 IP10 G12
2P51 D12 IP11 H12
2P52 D13 IP17 F13
2P53 D13 IP26 H5
2P54 D13 IP5U G6
2P55 D13 IP5V G7
2P56 F12 IP5Y G6
2P57 F12 IP5Z H6
2P58 G12 IP60 H13
2P59 G12
3P14 F13
3P34 E14
3P36 H6
3P38 H6
3P43 E9
3P47 H14
3P53 H5
3P58 B4
3P61 B4
3P63 D4
3P64 D4
3P65 I4
3P66 I4
3P67 F3
3P68 G3
3P75 G5
3P76 E9
3P77 E9
5P08 D12
5P11 B10
5P12 C10
5P13 C10
5P14 C10
5P15 H13
6P03 G13
7P01 A6
7P02 D10
7P12 H5
7P32 G6
9P0J G7
9P33 E9
BP1A F2
BP1B F1
BP1C F2
BP1D F1
BP1E F2
BP1F F1
BP1G F2
BP1H F2
BP1J A2
BP1K A2
BP1L A2
BP1M A2
BP1N A2
BP1P A2
BP1R B2
BP1S B2
BP1T B1
BP1U E1
BP1V G1
BP1W I1
BP5A C2
BP5B C2
BP5C C2
BP5D C2
BP5E D2
BP5F D2
BP5G D2
BP5H D2
BP5J H2
BP5K H2
BP5L H2
BP5M H2
BP5N I2
BP5P I2
BP5R I2
BP5S I2
FP03 F14
FP06 F1
FP07 F1
FP08 G1
FP09 G1
FP0A G1
FP0C G1
FP0E D1
FP0F D1
FP0G D2
FP0H D2
FP0J E1
FP0P D1
FP0R I1

CHN	SETNAME		
CLASS_NO	UFD2K8 DIGI IO TV543 R2 LDIPNX	8204 000 8934	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 8	130 – 4	A2
	CHECK DATE 2007-10-18		

18310_537_090303.eps
090303

SSB: HDMI Switch



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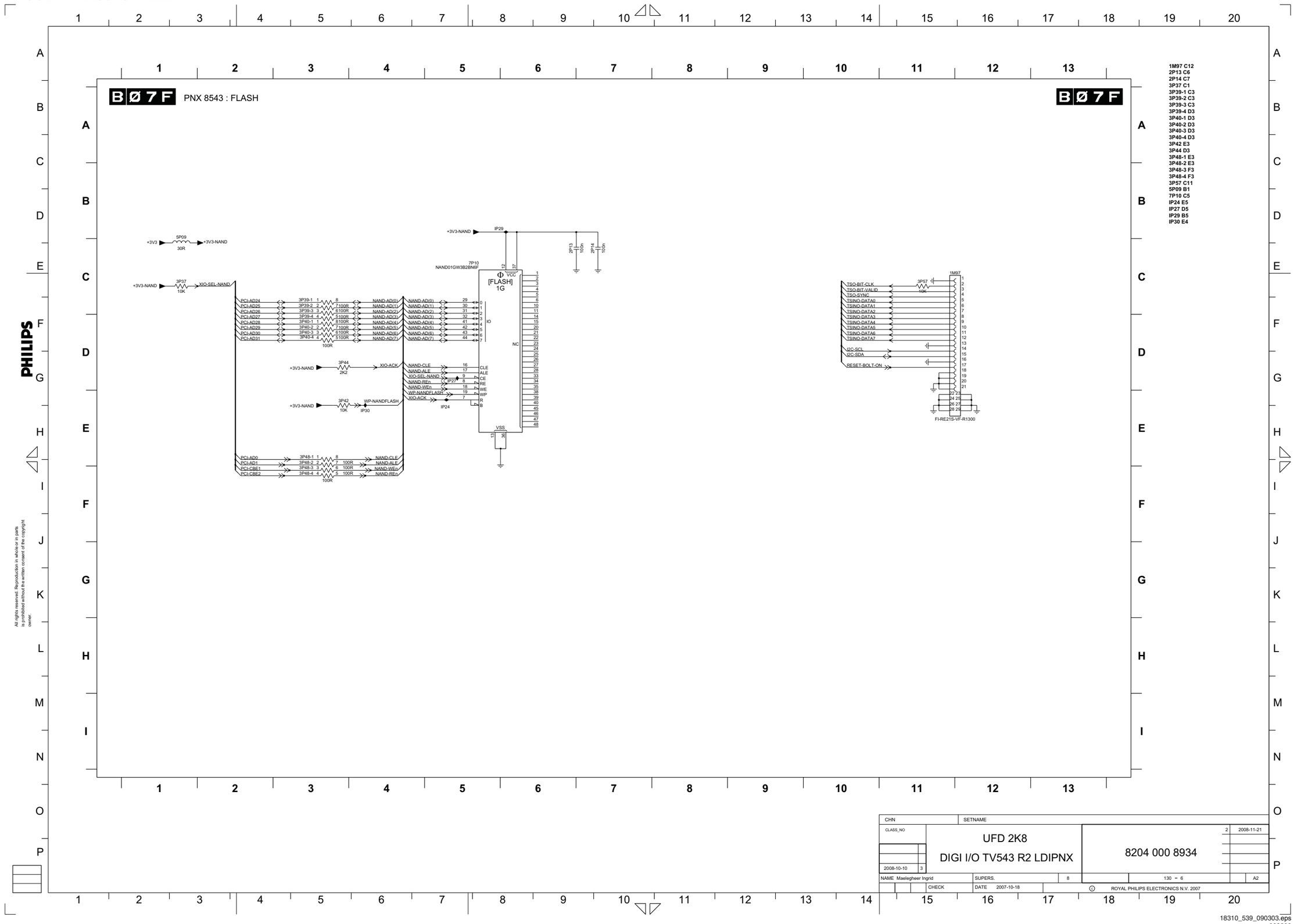
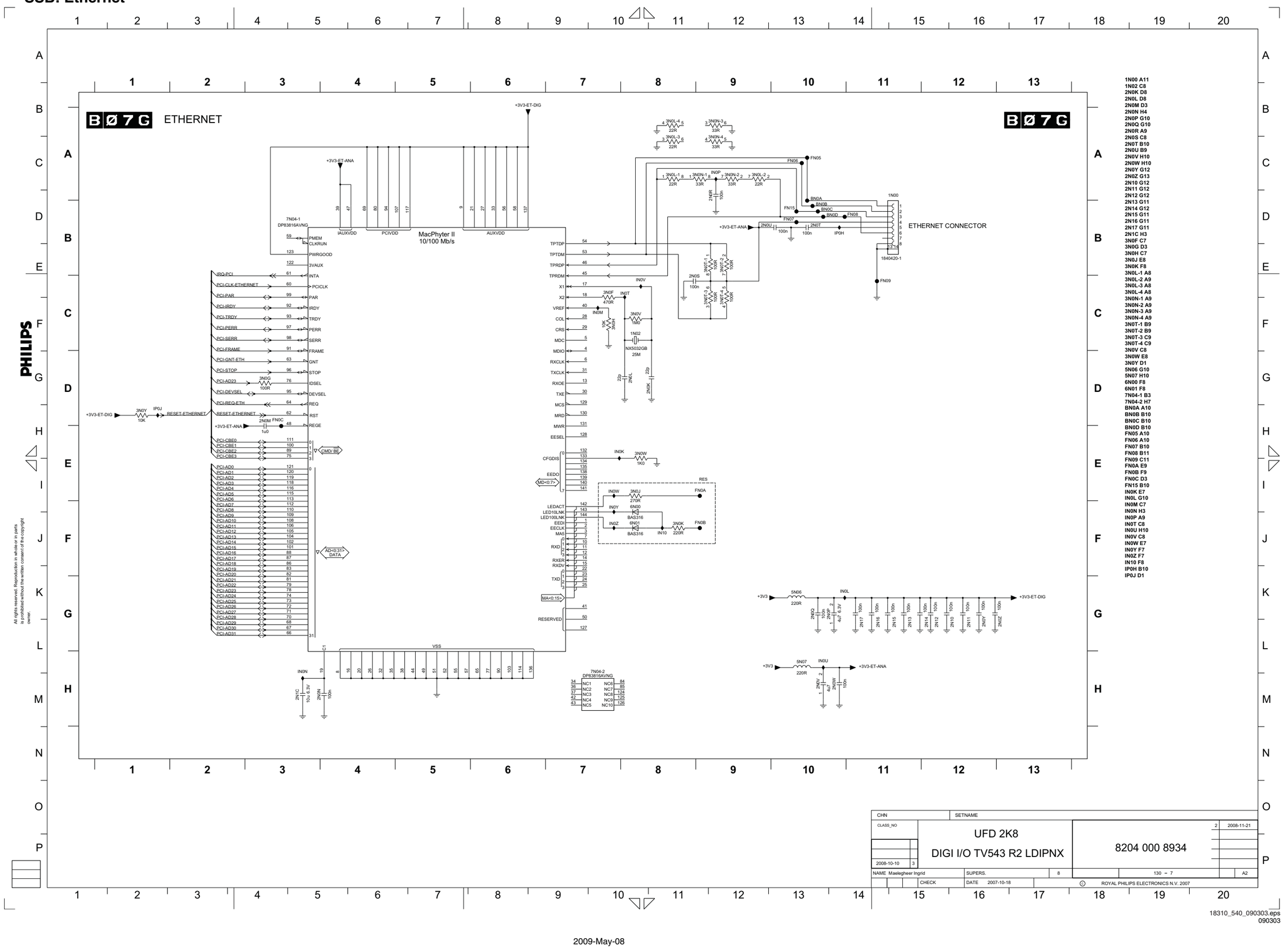
090303

SSB: PNX8543: Flash



SSB: Ethernet



1N00 A11
1N02 C8
2N0K D8
2N0L D8
2N0M D3
2N0N H4
2N0P G10
2N0Q G10
2N0R A9
2N0S C8
2N0T B10
2N0U B9
2N0V H10
2N0W H10
2N0Y G12
2N0Z G13
2N10 G12
2N11 G12
2N12 G12
2N13 G11
2N14 G12
2N15 G11
2N16 G11
2N17 G11
2N1C H3
3N0F C7
3N0G D3
3N0H C7
3N0J E8
3N0K F8
3N0L-1 A8
3N0L-2 A9
3N0L-3 A8
3N0L-4 A8
3N0N-1 A9
3N0N-2 A9
3N0N-3 A9
3N0N-4 A9
3N0T-1 B9
3N0T-2 B9
3N0T-3 C9
3N0T-4 C9
3N0V C8
3N0W E8
3N0Y D1
5N06 G10
5N07 H10
6N00 F8
6N01 F8
7N04-1 B3
7N04-2 H7
BN0A A10
BN0B B10
BN0C B10
BN0D B10
FN05 A10
FN06 A10
FN07 B10
FN08 B11
FN09 C11
FN0A E9
FN0B F9
FN0C D3
FN15 B10
IN0K E7
IN0L G10
IN0M C7
IN0N H3
IN0P A9
IN0T C8
IN0U H10
IN0V C8
IN0W E7
IN0Y F7
IN0Z F7
IN10 F8
IP0H B10
IP0J D1

CHN	SETNAME		
CLASS_NO	UFD 2K8 DIGI I/O TV543 R2 LDIPNX	8204 000 8934	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 8	130 – 7	A2
	CHECK DATE 2007-10-18	© ROYAL PHILIPS ELECTRONICS N.V. 2007	

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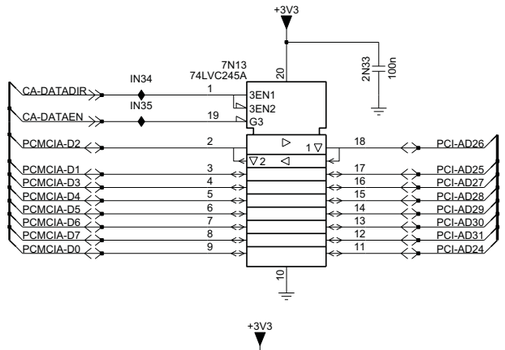
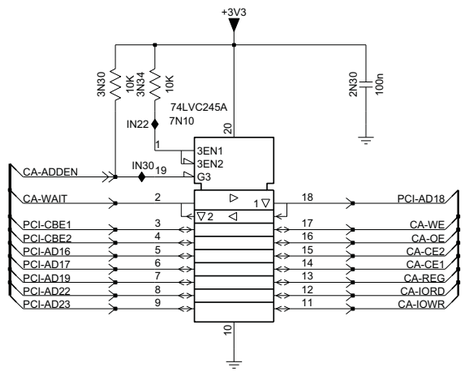
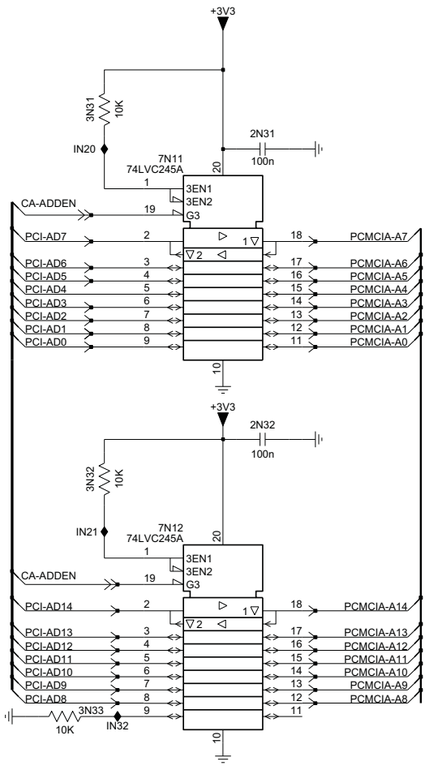
SSB: Buffering

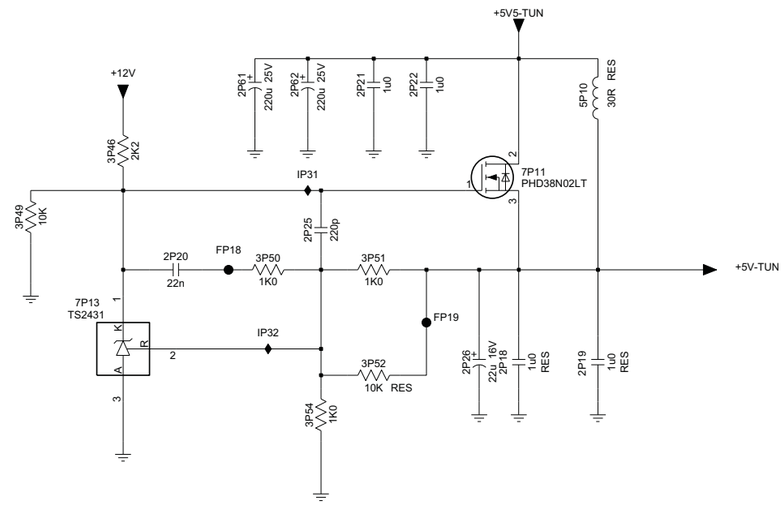
PHILIPS

BØ7H BUFFERING **BØ7H**









2N30 D3
2N31 B5
2N32 D5
2N33 B3
2P18 E9
2P19 E9
2P20 D7
2P21 C8
2P22 C8
2P25 D8
2P26 E9
2P61 C7
2P62 C8
3N30 D1
3N31 B4
3N32 D4
3N33 E4
3N34 D2
3P46 C7
3P49 D6
3P50 D8
3P51 D8
3P52 E8
3P54 E8
5P10 C9
7N10 D2
7N11 B5
7N12 D5
7N13 B2
7P11 D9
7P13 D7
FP18 D7
FP19 D8
IN20 B4
IN21 D4
IN22 D2
IN30 D2
IN32 E4
IN34 B2
IN35 B2
IP31 D8
IP32 D8

CHN	SETNAME		
CLASS_NO	UFD 2K8	2	2008-11-21
	DIGI I/O TV543 R2 LDIPNX	8204 000 8934	
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 8	130 – 8	A3
CHECK	DATE 2007-10-18	© ROYAL PHILIPS ELECTRONICS N.V. 2007	

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SSB: Analogue Externals A

B Ø 8 A ANALOGUE EXTERNALS A

B Ø 8 A

PHILIPS

SCART2 (AV2) 1E02

SCART1 (AV1) 1E01

MTJ-505H-01 NI LF

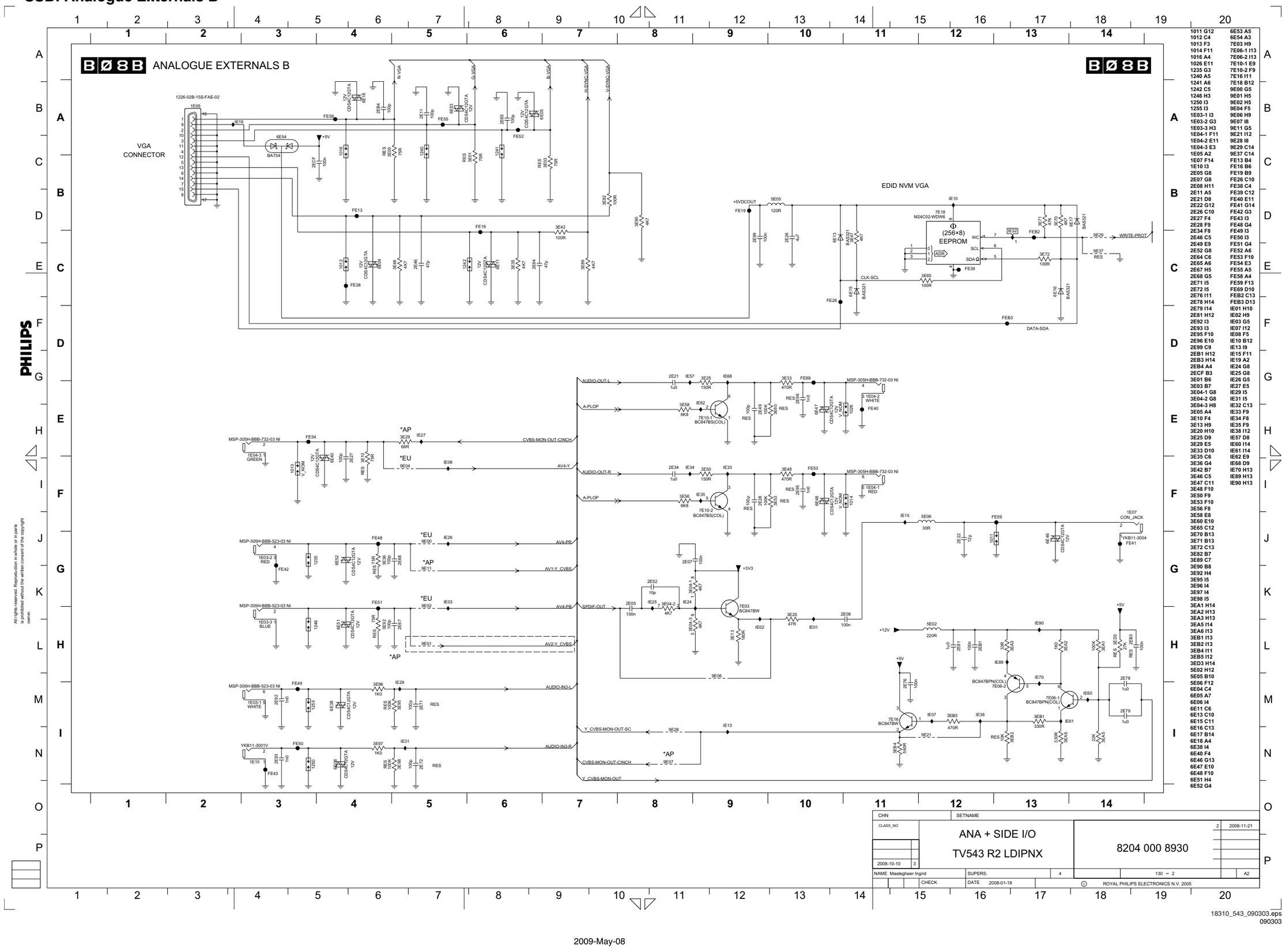
1001 E11	6E26 F12	2EA4 A3	FE84 F13
1009 B12	6E28 G12	2EA5 A3	FE85 F13
1015 C12	6E29 H12	3E02 D6	FEA0 A3
1022 A7	6E30 I11	3E06 D4	FEA1 B3
1023 B7	6E31 I6	3E07 A11	IE04 D1
1024 B7	6E32 I11	3E11 A6	IE05 D5
1025 C7	6E34 E6	3E12 A11	IE06 H6
1027 D6	6E35 F6	3E14 C6	IE09 H11
1028 E6	6E36 H7	3E15 B11	IE14 C5
1E00 A12	6E37 I6	3E16 D6	IE16 E5
1E01 C14	7E01-1 A2	3E17 E5	IE17 F5
1E02 C8	7E01-2 B2	3E18 B5	IE18 D10
1E12 D12	7E02 D2	3E19 C11	IE20 A5
1E13 E7	7E04 I1	3E21 B5	IE21 C5
1E16 F7	7E05 H1	3E22 C11	IE22 A11
1E18 F12	7E09 H11	3E24 A5	IE23 C11
1E19 G12	7E14 H5	3E27 B11	IE48 H11
1E22 H13	7E15 C3	3E28 D11	IE51 H5
1E23 I11	9E10 I3	3E30 B11	IE91 H1
1E24 I7	9E12 C5	3E31 D11	IE92 H2
1E25 I11	9E15 D5	3E32 E11	IE93 I2
1E26 H7	9E16 E5	3E34 C5	IE94 I1
1E27 I7	9E17 E5	3E37 A11	IE96 E2
1E31 B12	9E18 F5	3E38 F11	IE97 D3
2E01 A11	9E19 F5	3E43 H12	IE98 C2
2E04 C11	9E20 G10	3E44 H11	IEC0 A3
2E06 B11	9E22 D10	3E45 I10	IEC1 A2
2E10 B11	9E23 D10	3E51 E5	IEC2 A3
2E12 G12	9E24 E10	3E52 I5	IEC3 B2
2E13 G6	9E25 F10	3E54 G11	
2E14 F12	9E26 G10	3E55 F5	
2E15 D12	9E27 G10	3E59 I11	
2E16 D5	9E33 F2	3E61 H6	
2E17 E6	FE60 A7	3E62 I6	
2E18 E12	FE61 A7	3E63 A6	
2E19 F6	FE62 B7	3E64 B6	
2E24 H11	FE63 D7	3E68 H12	
2E29 A5	FE64 D7	3E69 H6	
2E30 B5	FE65 E7	3E73 G5	
2E31 C5	FE66 E7	3E99 C2	
2E32 B5	FE67 E7	3EA7 A3	
2E33 E5	FE68 C7	3EA8 A3	
2E41 I6	FE70 C13	3EA9 A2	
2E44 I12	FE71 C13	3EB0 B2	
2E50 A7	FE72 C13	3EB6 H1	
2E51 A7	FE73 D13	3EB7 H2	
2E70 B7	FE74 D13	3EB8 I2	
2E73 I2	FE75 D13	3EB9 I1	
2E74 G2	FE76 E7	6E01 A12	
2E75 D1	FE77 F7	6E02 E6	
2E77 C2	FE78 F7	6E03 B12	
2E82 C7	FE79 F7	6E07 B12	
2E87 A13	FE80 D13	6E08 B6	
2E88 A12	FE81 E13	6E09 C12	
2E90 B12	FE82 E13	6E10 A6	
2E91 C12	FE83 F13	6E12 B6	
		6E14 C6	
		6E22 E12	
		6E23 D11	
		6E24 D6	

1X04 EMC HOLE

CHN	SETNAME		
CLASS_NO	ANA + SIDE I/O TV543 R2 LDIPNX	8204 000 8930	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 4	130 – 1	A2
CHECK	DATE 2008-01-18	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

18310_542_090303.eps
090303

SSB: Analogue Externals B



1011 G12	6E53 A5
1012 C4	6E54 A3
1013 F3	7E03 H9
1014 F11	7E06-1 I13
1016 A4	7E06-2 I13
1026 E11	7E10-1 E9
1235 G3	7E10-2 F9
1240 A5	7E16 I11
1241 A6	7E18 B12
1242 C5	9E00 G5
1246 H3	9E01 H5
1250 I3	9E02 H5
1255 I3	9E04 F5
1E03-1 I3	9E06 H9
1E03-2 G3	9E07 I8
1E03-3 H3	9E11 G5
1E04-1 F11	9E21 I12
1E04-2 E11	9E28 I8
1E04-3 E3	9E29 C14
1E05 A2	9E37 C14
1E07 F14	9E13 B4
1E10 I3	9E16 B6
2E05 G8	FE19 B9
2E07 G8	FE26 C10
2E08 H11	FE38 C4
2E11 A5	FE39 C12
2E21 D8	FE40 E11
2E22 G12	FE41 G14
2E26 C10	FE42 G3
2E27 F4	FE43 I3
2E28 F9	FE48 G4
2E34 F8	FE49 I3
2E46 C5	FE50 I3
2E49 E9	FE51 G4
2E52 G8	FE52 A6
2E64 C6	FE53 F10
2E65 A6	FE54 E3
2E67 H5	FE55 A5
2E68 G5	FE58 A4
2E71 I5	FE59 F13
2E72 I5	FE69 D10
2E76 I11	FEB2 C13
2E78 H14	FEB3 D13
2E79 I14	IE01 H10
2E81 H12	IE02 H9
2E92 I3	IE03 G5
2E93 I3	IE07 I12
2E95 F10	IE08 F5
2E96 E10	IE10 B12
2E99 C9	IE13 I9
2EB1 H12	IE15 F11
2EB3 H14	IE19 A2
2EB4 A4	IE24 G8
2ECF B3	IE25 G8
3E01 B6	IE26 G5
3E03 B7	IE27 E5
3E04-1 G8	IE29 I5
3E04-2 G8	IE31 I5
3E04-3 H8	IE32 C13
3E05 A4	IE33 F9
3E10 F4	IE34 F8
3E13 H9	IE35 F9
3E20 H10	IE38 I12
3E25 D9	IE57 D8
3E29 E5	IE60 I14
3E33 D10	IE61 I14
3E35 C6	IE62 E9
3E36 G4	IE68 D9
3E42 B7	IE70 H13
3E46 C5	IE89 H13
3E47 C11	IE90 H13
3E48 F10	
3E50 F9	
3E53 F10	
3E56 F8	
3E58 E8	
3E60 E10	
3E65 C12	
3E70 B13	
3E71 B13	
3E72 C13	
3E82 B7	
3E89 C7	
3E90 B8	
3E92 H4	
3E95 I5	
3E96 I4	
3E97 I4	
3E98 I5	
3EA1 H14	
3EA2 H13	
3EA3 H13	
3EA5 I14	
3EA6 I13	
3EB1 I13	
3EB2 I13	
3EB4 I11	
3EB5 I12	
3ED3 H14	
5E02 H12	
5E05 B10	
5E06 F12	
6E04 C4	
6E05 A7	
6E06 I4	
6E11 C6	
6E13 C10	
6E15 C11	
6E16 C13	
6E17 B14	
6E18 A4	
6E38 I4	
6E40 F4	
6E46 G13	
6E47 E10	
6E48 F10	
6E51 H4	
6E52 G4	

CHN	SETNAME		
CLASS_NO	ANA + SIDE I/O TV543 R2 LDIPNX	8204 000 8930	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 4	130 – 2	A2
CHECK	DATE 2008-01-18	© ROYAL PHILIPS ELECTRONICS N.V. 2005	

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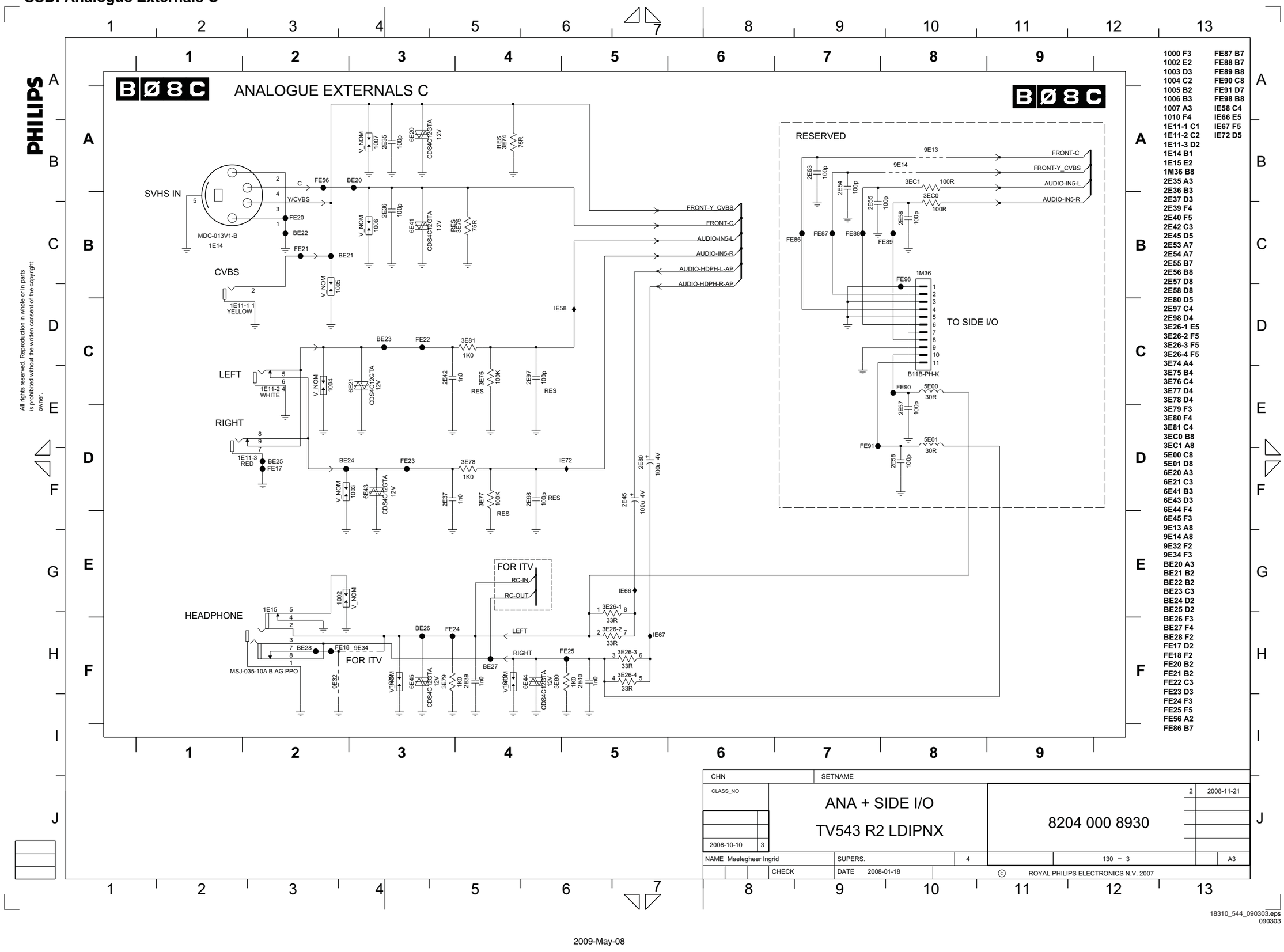
SSB: Analogue Externals C



1000 F3 FE87 B7
1002 E2 FE88 B7
1003 D3 FE89 B8
1004 C2 FE90 C8
1005 B2 FE91 D7
1006 B3 FE98 B8
1007 A3 IE58 C4
1010 F4 IE66 E5
1E11-1 C1 IE67 F5
1E11-2 C2 IE72 D5
1E11-3 D2
1E14 B1
1E15 E2
1M36 B8
2E35 A3
2E36 B3
2E37 D3
2E39 F4
2E40 F5
2E42 C3
2E45 D5
2E53 A7
2E54 A7
2E55 B7
2E56 B8
2E57 D8
2E58 D8
2E80 D5
2E97 C4
2E98 D4
3E26-1 E5
3E26-2 F5
3E26-3 F5
3E26-4 F5
3E74 A4
3E75 B4
3E76 C4
3E77 D4
3E78 D4
3E79 F3
3E80 F4
3E81 C4
3EC0 B8
3EC1 A8
5E00 C8
5E01 D8
6E20 A3
6E21 C3
6E41 B3
6E43 D3
6E44 F4
6E45 F3
9E13 A8
9E14 A8
9E32 F2
9E34 F3
BE20 A3
BE21 B2
BE22 B2
BE23 C3
BE24 D2
BE25 D2
BE26 F3
BE27 F4
BE28 F2
FE17 D2
FE18 F2
FE20 B2
FE21 B2
FE22 C3
FE23 D3
FE24 F3
FE25 F5
FE56 A2
FE86 B7

CHN	SETNAME		
CLASS_NO	ANA + SIDE I/O	2	2008-11-21
	TV543 R2 LDIPNX		
2008-10-10 3		8204 000 8930	
NAME Maelegheer Ingrid	SUPERS. 4	130 – 3	A3
CHECK	DATE 2008-01-18		

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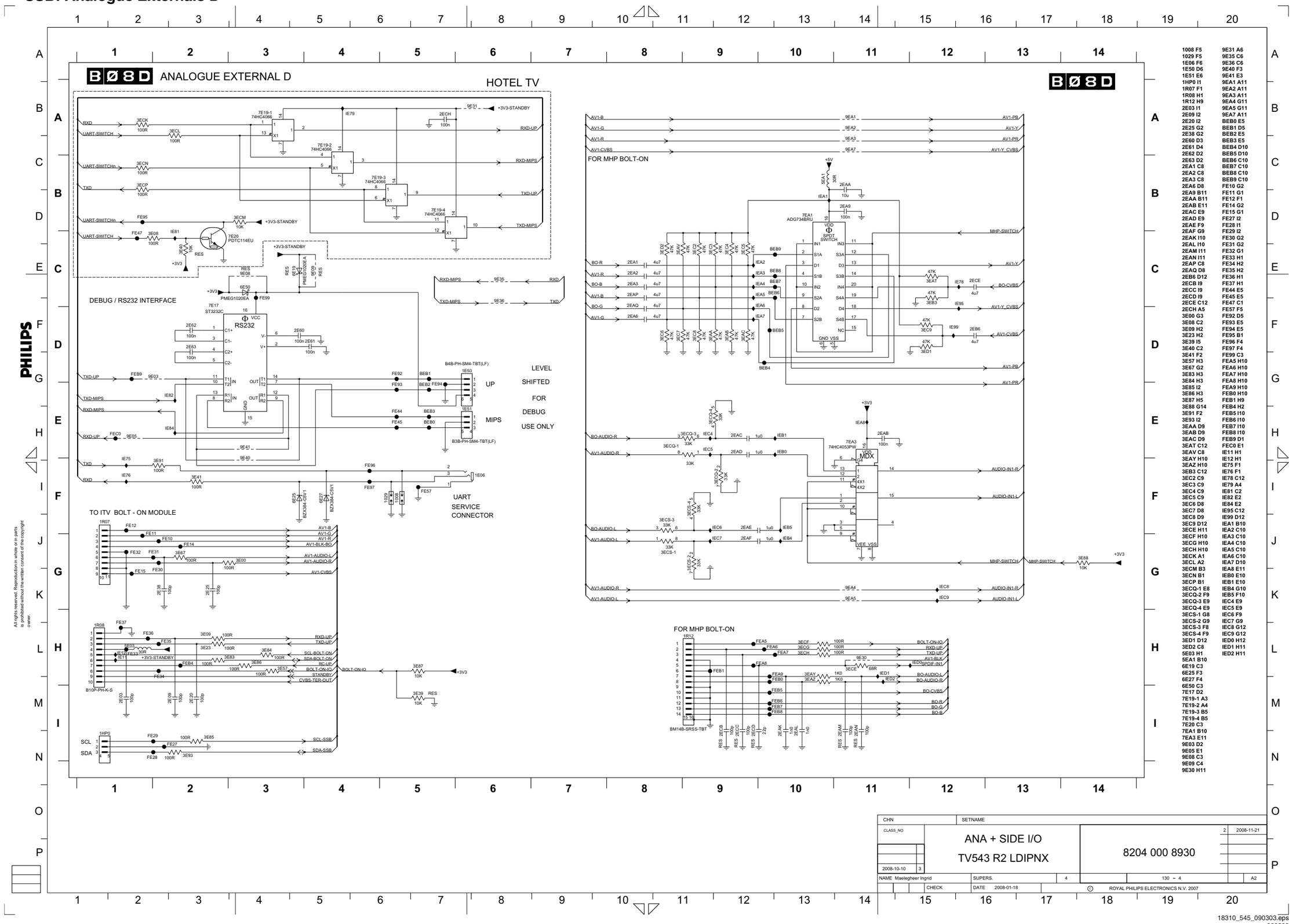
SSB: Analogue Externals D



1008 F5 9E31 A6
1029 F5 9E35 C6
1E06 F6 9E36 C6
1E50 D6 9E40 F3
1E51 E6 9E41 E3
1HP0 I1 9EA1 A11
1R07 F1 9EA2 A11
1R08 H1 9EA3 A11
1R12 H9 9EA4 G11
2E03 I1 9EA5 G11
2E09 I2 9EA7 A11
2E20 I2 BEB0 E5
2E25 G2 BEB1 D5
2E38 G2 BEB2 E5
2E60 D3 BEB3 E5
2E61 D4 BEB4 D10
2E62 D2 BEB5 D10
2E63 D2 BEB6 C10
2EA1 C8 BEB7 C10
2EA2 C8 BEB8 C10
2EA3 C8 BEB9 C10
2EA6 D8 FE10 G2
2EA9 B11 FE11 G1
2EAA B11 FE12 F1
2EAB E11 FE14 G2
2EAC E9 FE15 G1
2EAD E9 FE27 I2
2EAE F9 FE28 I1
2EAF G9 FE29 I2
2EAK I10 FE30 G2
2EAL I10 FE31 G2
2EAM I11 FE32 G1
2EAN I11 FE33 H1
2EAP C8 FE34 H2
2EAQ D8 FE35 H2
2EB6 D12 FE36 H1
2ECB I9 FE37 H1
2ECC I9 FE44 E5
2ECD I9 FE45 E5
2ECE C12 FE47 C1
2ECH A5 FE57 F5
3E00 G3 FE92 D5
3E08 C2 FE93 E5
3E09 H2 FE94 E5
3E23 H2 FE95 B1
3E39 I5 FE96 F4
3E40 C2 FE97 F4
3E41 F2 FE99 C3
3E57 H3 FEA5 H10
3E67 G2 FEA6 H10
3E83 H3 FEA7 H10
3E84 H3 FEA8 H10
3E85 I2 FEA9 H10
3E86 H3 FEB0 H10
3E87 H5 FEB1 H9
3E88 G14 FEB4 H2
3E91 F2 FEB5 I10
3E93 I2 FEB6 I10
3EAA D9 FEB7 I10
3EAB D9 FEB8 I10
3EAC D9 FEB9 D1
3EAT C12 FEC0 E1
3EAV C8 IE11 H1
3EAY H10 IE12 H1
3EAZ H10 IE75 F1
3EB3 C12 IE76 F1
3EC2 C9 IE78 C12
3EC3 C9 IE79 A4
3EC4 C9 IE81 C2
3EC5 C9 IE82 E2
3EC6 D8 IE84 E2
3EC7 D8 IE95 C12
3EC8 D9 IE99 D12
3EC9 D12 IEA1 B10
3ECE H11 IEA2 C10
3ECF H10 IEA3 C10
3ECG H10 IEA4 C10
3ECH H10 IEA5 C10
3ECK A1 IEA6 C10
3ECL A2 IEA7 D10
3ECM B3 IEA8 E11
3ECN B1 IEB0 E10
3ECP B1 IEB1 E10
3ECQ-1 E8 IEB4 G10
3ECQ-2 F9 IEB5 F10
3ECQ-3 E9 IEC4 E9
3ECQ-4 E9 IEC5 E9
3ECS-1 G8 IEC6 F9
3ECS-2 G9 IEC7 G9
3ECS-3 F8 IEC8 G12
3ECS-4 F9 IEC9 G12
3ED1 D12 IED0 H12
3ED2 C8 IED1 H11
5E03 H1 IED2 H11
5EA1 B10
6E19 C3
6E25 F3
6E27 F4
6E50 C3
7E17 D2
7E19-1 A3
7E19-2 A4
7E19-3 B5
7E19-4 B5
7E20 C3
7EA1 B10
7EA3 E11
9E03 D2
9E05 E1
9E08 C3
9E09 C4
9E30 H11

CHN	SETNAME		
CLASS_NO	ANA + SIDE I/O TV543 R2 LDIPNX	8204 000 8930	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 4	130 – 4	A2
CHECK	DATE 2008-01-18		

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SSB: Mini PCI Connector

B Ø 9A MINI PCI CONNECTOR

B Ø 9A

+3V3 — 5A00 30R — IA28 — +3V3-mPCI

RES 2A00 1* 330u 6.3V; 2A01 1u0; 2A02 100n; 2A03 100n; 2A04 100n; 2A05 100n; 2A06 100n; 2A07 100n; 2A08 100n; 2A09 100n

RES
+5V — 5A01 30R — FA37 — +5V-mPCI
2A50 1u0; 2A51 100n; 2A52 100n

ROW_A 1A01-A

IRQB-mPCI — IA29 — 9A00 RES — IRQ-PCI
+3V3-mPCI
PCI-CLK-MINI
PCI-REQ-MINI
+3V3-mPCI
PCI-AD31
PCI-AD29
PCI-AD27
PCI-AD25
PCI-CBE3
PCI-AD23
PCI-AD21
PCI-AD19
PCI-AD17
PCI-CBE2
PCI-IRDY
+3V3-mPCI
PCI-CLKRUN — PCI-CLKRUN — IA30 — 3A01 10K
PCI-SERR
PCI-PERR
PCI-CBE1
PCI-AD14
PCI-AD12
PCI-AD10
PCI-AD8
PCI-AD7
+3V3-mPCI
PCI-AD5
PCI-AD3
+5V-mPCI
PCI-AD1
FA30
FA31
FA32
FA33
1734065-3

ROW_B 1A01-B

+5V-mPCI — IA27 — 9A01 — IRQ-PCI
IRQA-mPCI
IA26
RESET-mPCI — RESET-mPCI — 9A02 — RESET-ETHERNET
+3V3-mPCI
PCI-GNT-MINI
PME — PME — IA20 — 3A02 10K — +3V3-mPCI
PCI-AD30
+3V3-mPCI
PCI-AD28
PCI-AD26
PCI-AD24
IDSEL
PCI-AD22
PCI-AD20
PCI-PAR
PCI-AD18
PCI-AD16
PCI-FRAME
PCI-TRDY
PCI-STOP
+3V3-mPCI
PCI-DEVSEL
PCI-AD15
PCI-AD13 — PCI-AD13 — IA21 — 3A05 — IDSEL
PCI-AD11 — PCI-AD11 — IA22 — 3A04 100R RES — 100R
PCI-AD9
PCI-CBE0
+3V3-mPCI
PCI-AD12 — IA23 — 3A03 RES 100R
PCI-AD6
PCI-AD4
PCI-AD2
PCI-AD0
M66EN — M66EN — IA24 — 3A00 10K
FA34
FA35
FA36
MPCIACT — MPCIACT — IA25 — 3A06 10K — +3V3-mPCI
125
1734065-3

1X09 REF EMC HOLE

1A01-A A1
1A01-B A6
2A00 A3
2A01 A3
2A02 A3
2A03 A3
2A04 A4
2A05 A4
2A06 A4
2A07 A4
2A08 A5
2A09 A5
2A50 A7
2A51 A7
2A52 A8
3A00 E9
3A01 C4
3A02 B9
3A03 D9
3A04 D9
3A05 D9
3A06 E9
5A00 A2
5A01 A7
9A00 B3
9A01 B7
9A02 B9
FA30 E1
FA31 E2
FA32 E1
FA33 E1
FA34 E6
FA35 E6
FA36 E6
FA37 A8
IA20 B9
IA21 D9
IA22 D9
IA23 D9
IA24 E9
IA25 E9
IA26 B7
IA27 B7
IA28 A3
IA29 B2
IA30 C4

CHN	SETNAME		
CLASS_NO	MINI PCI TV543 R2 LDIPNX	8204 000 8935	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 2	130 – 1	A3
CHECK	DATE 2007-10-16	© ROYAL PHILIPS ELECTRONICS N.V. 2008	

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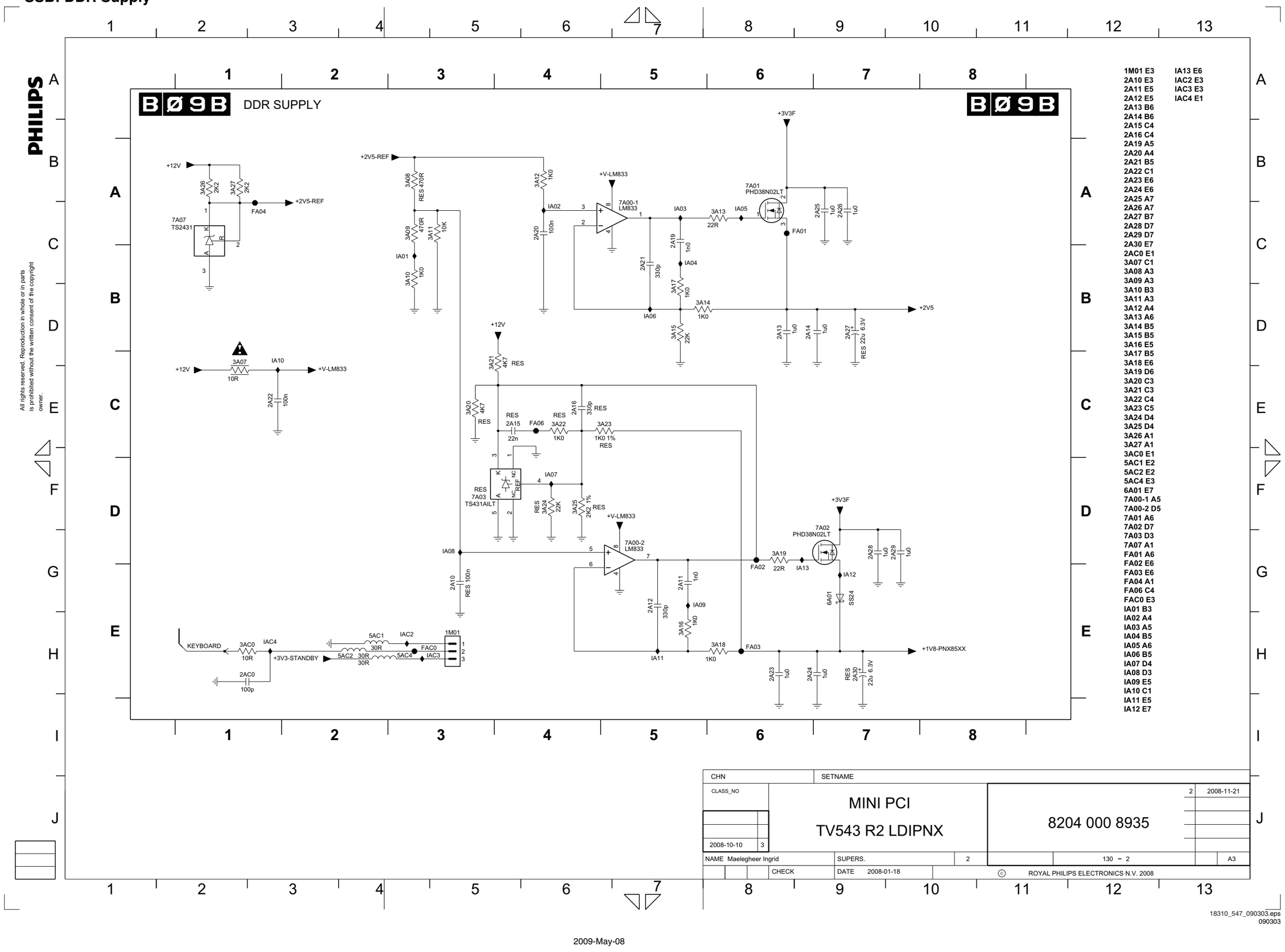
SSB: DDR Supply



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CLASS_NO	MINI PCI TV543 R2 LDIPNX	8204 000 8935	2 2008-11-21
2008-10-10 3			
NAME Maelegheer Ingrid	SUPERS. 2	130 – 2	A3
CHECK	DATE 2008-01-18		

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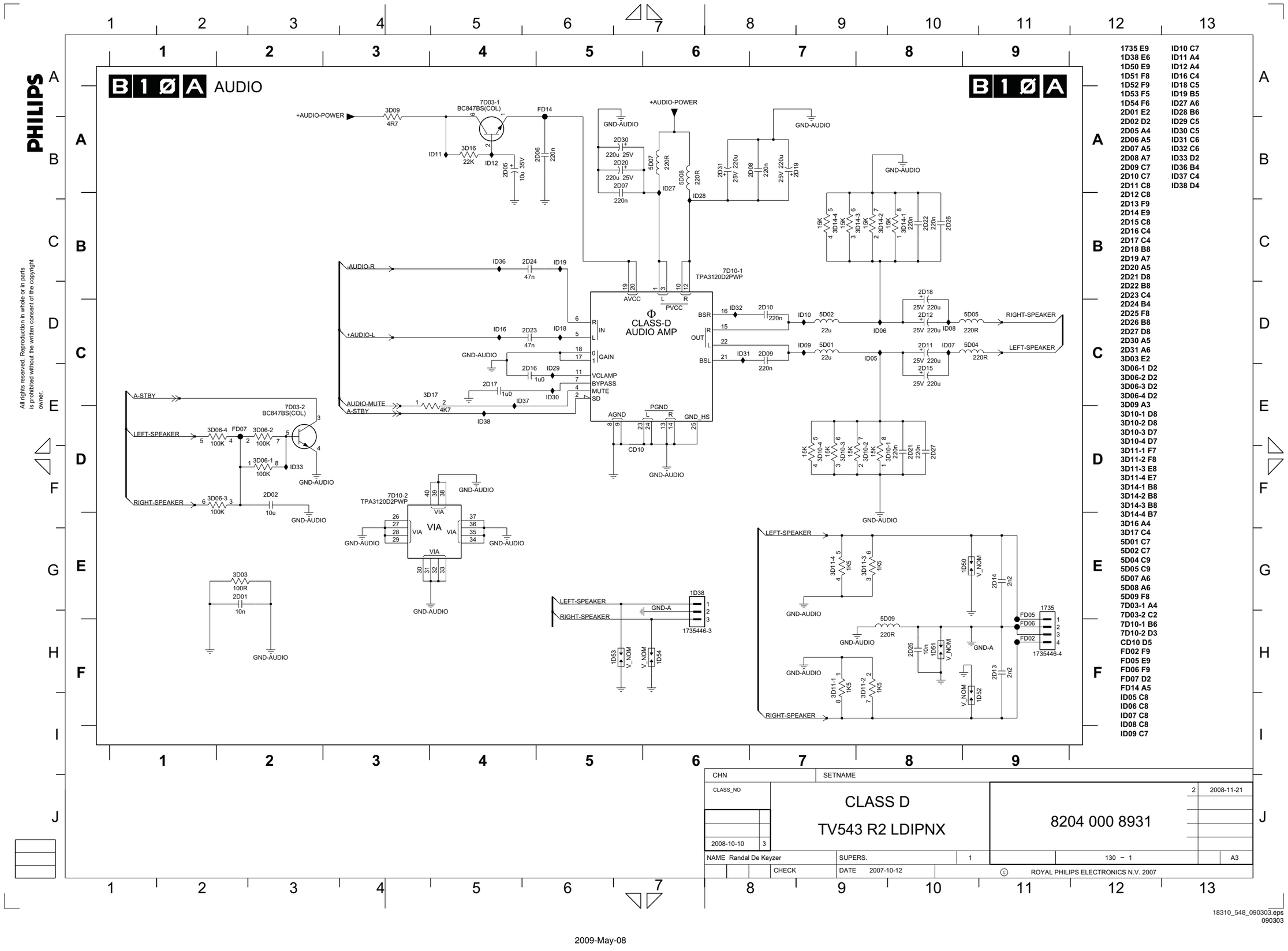
SSB: Audio



1735 E9
1D38 E6
1D50 E9
1D51 F8
1D52 F9
1D53 F5
1D54 F6
2D01 E2
2D02 D2
2D05 A4
2D06 A5
2D07 A5
2D08 A7
2D09 C7
2D10 C7
2D11 C8
2D12 C8
2D13 F9
2D14 E9
2D15 C8
2D16 C4
2D17 C4
2D18 B8
2D19 A7
2D20 A5
2D21 D8
2D22 B8
2D23 C4
2D24 B4
2D25 F8
2D26 B8
2D27 D8
2D30 A5
2D31 A6
3D03 E2
3D06-1 D2
3D06-2 D2
3D06-3 D2
3D06-4 D2
3D09 A3
3D10-1 D8
3D10-2 D8
3D10-3 D7
3D10-4 D7
3D11-1 F7
3D11-2 F8
3D11-3 E8
3D11-4 E7
3D14-1 B8
3D14-2 B8
3D14-3 B8
3D14-4 B7
3D16 A4
3D17 C4
5D01 C7
5D02 C7
5D04 C9
5D05 C9
5D07 A6
5D08 A6
5D09 F8
7D03-1 A4
7D03-2 C2
7D10-1 B6
7D10-2 D3
CD10 D5
FD02 F9
FD05 E9
FD06 F9
FD07 D2
FD14 A5
ID05 C8
ID06 C8
ID07 C8
ID08 C8
ID09 C7
ID10 C7
ID11 A4
ID12 A4
ID16 C4
ID18 C5
ID19 B5
ID27 A6
ID28 B6
ID29 C5
ID30 C5
ID31 C6
ID32 C6
ID33 D2
ID36 B4
ID37 C4
ID38 D4

CHN	SETNAME		
CLASS_NO	CLASS D TV543 R2 LDIPNX	2	2008-11-21
2008-10-10 3		8204 000 8931	
NAME Randal De Keyzer	SUPERS. 1	130 – 1	A3
	CHECK DATE 2007-10-12	© ROYAL PHILIPS ELECTRONICS N.V. 2007	

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SSB: SRP List Explanation

Example

Net Name	Diagram
+12-15V	AP1 (4x)
+12-15V	AP4 (4x)
+12-15V	AP5 (12x)
+12-15V	AP6 (4x)
+12-15V	AP7 (8x)
+12V	AP1 (4x)
+12V_NF	AP1 (2x)
+12VAL	AP1 (2x)
+25VLP	AP1 (4x)
+25VLP	AP2 (1x)
+3V3-STANDBY	AP5 (3x)
+400V-F	AP1 (2x)
+400V-F	AP2 (2x)
+400V-F	AP3 (2x)
+5V2	AP1 (6x)
+5V2	AP2 (1x)
+5V2-NF	AP1 (1x)
+5V2-NF	AP2 (1x)
+5V-SW	AP1 (6x)
+5V-SW	AP2 (1x)
+8V6	AP1 (3x)
+AUX	AP1 (2x)
+AUX	AP2 (1x)
+DC-F	AP1 (2x)
+DC-F	AP3 (2x)
+SUB-SPEAKER	AP5 (1x)
+SUB-SPEAKER	AP6 (2x)
-12-15V	AP1 (4x)
-12-15V	AP4 (6x)
-12-15V	AP5 (14x)
-12-15V	AP6 (6x)
-12-15V	AP7 (8x)
AL-OFF	AP1 (2x)
AUDIO-L	AP4 (1x)
AUDIO-L	AP5 (1x)
AUDIO-PROT	AP5 (3x)
AUDIO-R	AP4 (1x)
AUDIO-R	AP5 (1x)
AUDIO-SW	AP5 (1x)
AUDIO-SW	AP7 (1x)
BOOST	AP1 (2x)
CPROT	AP4 (2x)
CPROT	AP5 (1x)
CPROT-SW	AP5 (1x)
CPROT-SW	AP6 (2x)
-DC-F	AP1 (2x)
-DC-F	AP3 (2x)
DC-PROT	AP1 (1x)
DC-PROT	AP5 (2x)
DIM-CONTROL	AP1 (2x)
FEEDBACK+SW	AP6 (2x)
FEEDBACK-L	AP4 (2x)
FEEDBACK-R	AP4 (2x)
FEEDBACK-SW	AP6 (2x)
GND-AL	AP1 (2x)
GNDHA	AP1 (40x)
GNDHA	AP2 (20x)
GNDHA	AP3 (2x)
GNDHOT	AP3 (2x)
GND-L	AP1 (2x)
GND-L	AP4 (4x)
GND-L	AP5 (34x)
GND-LL	AP4 (7x)
GND-LL	AP5 (1x)
GND-LR	AP4 (7x)
GND-LR	AP5 (1x)
GND-LSW	AP5 (1x)
GND-LSW	AP6 (15x)
GND-S	AP1 (11x)
GND-SA	AP4 (8x)
GND-SA	AP5 (2x)
GND-SA	AP6 (8x)
GND-SA	AP7 (6x)
GNDscrew	AP3 (2x)
GNDscrew	AP5 (2x)
GND-SSB	AP5 (3x)
GND-SSP	AP1 (51x)
GND-SSP	AP2 (15x)
IN+SW	AP6 (2x)
IN-L	AP4 (2x)
IN-R	AP4 (2x)
IN-SW	AP6 (2x)
INV-MUTE	AP4 (1x)
INV-MUTE	AP5 (1x)
INV-MUTE	AP6 (1x)
LEFT-SPEAKER	AP4 (1x)
LEFT-SPEAKER	AP5 (1x)
MUTE	AP4 (2x)
MUTE	AP5 (1x)
MUTE	AP6 (2x)
ON-OFF	AP1 (3x)
OUT	AP6 (1x)
OUT	AP7 (2x)
OUTN	AP6 (1x)
OUTN	AP7 (1x)
POWER-GOOD	AP1 (2x)
POWER-OK-PLATFORM	AP1 (2x)
RIGHT-SPEAKER	AP4 (1x)
RIGHT-SPEAKER	AP5 (1x)
SOUND-ENABLE	AP5 (3x)
STANDBY	AP1 (5x)
STANDBY	AP2 (1x)
-SUB-SPEAKER	AP5 (1x)
-SUB-SPEAKER	AP6 (2x)
V-CLAMP	AP1 (1x)
V-CLAMP	AP3 (2x)

1.1. Introduction

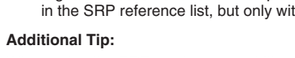
SRP (Service Reference Protocol) is a software tool that creates a list with all references to signal lines. The list contains references to the signals within all schematics of a PWB. It replaces the text references currently printed next to the signal names in the schematics. These printed references are created manually and are therefore not guaranteed to be 100% correct. In addition, in the current crowded schematics there is often none or very little place for these references.
Some of the PWB schematics will use SRP while others will still use the manual references. Either there will be an SRP reference list for a schematic, or there will be printed references in the schematic.

1.2. Non-SRP Schematics

There are several different signals available in a schematic:

1.2.1. Power Supply Lines

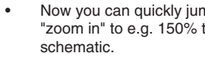
All power supply lines are available in the supply line overview (see chapter 6). In the schematics (see chapter 7) is not indicated where supplies are coming from or going to.
It is however indicated if a supply is incoming (created elsewhere), or outgoing (created or adapted in the current schematic).



Outgoing Incoming

1.2.2. Normal Signals

For normal signals, a schematic reference (e.g. B14b) is placed next to the signals.

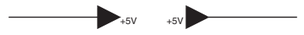


1.2.3. Grounds

For normal and special grounds (e.g. GNDHOT or GND3V3 etc.), nothing is indicated.

1.3. SRP Schematics

SRP is a tool, which automatically creates a list with signal references, indicating on which schematic the signals are used.
A reference is created for all signals indicated with an SRP symbol, these symbols are:



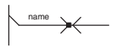
Power supply line.

Stand alone signal or switching line (used as less as possible).

Signal line into a wire tree.

Switching line into a wire tree.

Bi-directional line (e.g. SDA) into a wire tree.



Signal line into a wire tree, its direction depends on the circuit (e.g. ingoing for PDP, outgoing for LCD sets).

Remarks:

- When there is a black dot on the "signal direction arrow" it is an SRP symbol, so there will be a reference to the signal name in the SRP list.
- All references to normal grounds (Ground symbols without additional text) are not listed in the reference list, this to keep it concise.
- Signals that are not used in multiple schematics, but only once or several times in the same schematic, are included in the SRP reference list, but only with one reference.

Additional Tip:

When using the PDF service manual file, you can very easily search for signal names and follow the signal over all the schematics. In Adobe PDF reader:

- Select the signal name you want to search for, with the "Select text" tool.
- Copy and paste the signal name in the "Search PDF" tool.
- Search for all occurrences of the signal name.
- Now you can quickly jump between the different occurrences and follow the signal over all schematics. It is advised to "zoom in" to e.g. 150% to see clearly, which text is selected. Then you can zoom out, to get an overview of the complete schematic.

PS. It is recommended to use at least Adobe PDF (reader) version 6.x, due to better search possibilities in this version.

10000_031_090121.eps
090121

Personal Notes:

SSB: SRP List Part 1

Netname	Schematic
B01B	+12V
B01C	+12V
B02B	+12V
B06B	+12V
B06C	+12V
B07B	+12V
B07H	+12V
B08B	+12V
B09B	+12V
B01B	+12VD
B05H	+12VD
B01A	+12VF
B01B	+12VF
B01A	+12VF1
B01C	+12VF2
B02B	+1V2
B02B	+1V2A
B06E	+1V2-FPGA
B06G	+1V2-FPGA
B06A	+1V2M
B06E	+1V2-PLL
B06G	+1V2-PLL
B01C	+1V2-PNX5100
B04A	+1V2-PNX5100
B05C	+1V2-PNX5100
B05C	+1V2-PNX5100-CLOCK
B05C	+1V2-PNX5100-DDR-PLL1
B05C	+1V2-PNX5100-DLL
B05C	+1V2-PNX5100-LVDS-PLL
B05C	+1V2-PNX5100-TRI-PLL1
B05C	+1V2-PNX5100-TRI-PLL2
B05C	+1V2-PNX5100-TRI-PLL3
B01A	+1V2-PNX85XX
B02B	+1V2-PNX85XX
B04A	+1V2-PNX85XX
B04P	+1V2-PNX85XX
B06A	+1V2-PNX85XX
B06E	+1V2-PNX85XX
B01A	+1V2-STANDBY
B01B	+1V2-STANDBY
B04P	+1V2-STANDBY
B05A	+1V8-PNX5100
B05C	+1V8-PNX5100
B06E	+1V8-PNX5100
B04G	+1V8-PNX85XX
B04P	+1V8-PNX85XX
B06E	+1V8-PNX85XX
B07D	+1V8-PNX85XX
B09B	+1V8-PNX85XX
B06A	+2V5
B06E	+2V5
B06F	+2V5
B09B	+2V5
B06F	+2V5-DDR1
B06G	+2V5-DDR1
B06E	+2V5in-FPGA
B06G	+2V5in-FPGA
B06A	+2V5M
B06E	+2V5out-FPGA
B06G	+2V5out-FPGA
B06E	+2V5-PLL
B06G	+2V5-PLL
B09B	+2V5-REF
B01B	+33VTUN
B02A	+33VTUN
B01A	+3V3
B01B	+3V3
B02B	+3V3
B04A	+3V3
B04L	+3V3
B04M	+3V3
B04N	+3V3
B04P	+3V3
B05C	+3V3
B05E	+3V3
B05F	+3V3
B05G	+3V3
B05H	+3V3
B05I	+3V3
B06A	+3V3
B06B	+3V3
B06C	+3V3
B06E	+3V3
B07A	+3V3
B07C	+3V3
B07D	+3V3
B07F	+3V3
B07G	+3V3
B07H	+3V3
B08A	+3V3
B08B	+3V3
B08D	+3V3
B09A	+3V3
B02A	+3V3A
B02B	+3V3A
B02B	+3V3D
B02B	+3V3E
B07G	+3V3-ET-ANA
B07G	+3V3-ET-DIG
B01A	+3V3F
B05H	+3V3F
B09B	+3V3F
B06E	+3V3-FPGA
B06G	+3V3-FPGA
B06A	+3V3M
B09A	+3V3-mPCI
B07F	+3V3-NAND
B04A	+3V3-PER
B04B	+3V3-PER
B04E	+3V3-PER
B04F	+3V3-PER
B04N	+3V3-PER
B04P	+3V3-PER
B05C	+3V3-PNX5100-CLOCK
B05C	+3V3-PNX5100-DDR-PLL0
B05C	+3V3-PNX5100-LVDS-IN
B05C	+3V3-PNX5100-LVDS-PLL
B01B	+3V3-STANDBY
B04A	+3V3-STANDBY
B04P	+3V3-STANDBY
B07D	+3V3-STANDBY
B08D	+3V3-STANDBY
B09B	+3V3-STANDBY
B01B	+5V
B01C	+5V
B04A	+5V
B04L	+5V
B06A	+5V
B07C	+5V
B07D	+5V
B08A	+5V
B08B	+5V
B08D	+5V
B09A	+5V
B01C	+5V5-TUN
B07H	+5V5-TUN
B07E	+5V-DDC
B07D	+5V-EDID
B07E	+5V-EDID
B09A	+5V-mPCI
B02A	+5V-TUN
B02B	+5V-TUN
B07H	+5V-TUN
B02B	+5V-TUN-CVBS
B02A	+5V-TUN-PIN
B04I	+AUDIO-L
B10	+AUDIO-L
B01B	+AUDIO-POWER
B04I	+AUDIO-POWER
B04M	+AUDIO-POWER
B10	+AUDIO-POWER
B05H	+VDISP
B06D	+VDISP
B05E	+VDISP1
B05H	+VDISP1
B05E	+VDISP2
B05H	+VDISP2
B09B	+V-LM833
B02A	+VTUN
B07D	1V8-HDMI
B04I (1x)	ADAC(1)
B04L (1x)	ADAC(1)
B04I (1x)	ADAC(2)
B04L (1x)	ADAC(2)
B04L (1x)	ADAC(3)
B04M (1x)	ADAC(3)
B04L (1x)	ADAC(4)
B04M (1x)	ADAC(4)
B04I (1x)	ADAC(5)
B04L (1x)	ADAC(5)
B04I (1x)	ADAC(6)
B04L (1x)	ADAC(6)
B04I (1x)	ADAC(7)
B04L (3x)	ADAC(7)
B04I (1x)	ADAC(8)
B04L (3x)	ADAC(8)
B07D (4x)	AIN-5V
B04A (2x)	ALE
B05D (1x)	AMBI-VS
B02B (2x)	ANTENNA-CTRL
B02A (2x)	ANTENNA-SUPPLY
B02B (1x)	ANTENNA-SUPPLY
B04M (1x)	A-PLOP
B08A (1x)	A-PLOP
B08B (2x)	A-PLOP
B08A (3x)	AP-SCART-OUT-L
B08A (3x)	AP-SCART-OUT-R
B07D (2x)	ARX0-
B07D (2x)	ARX0+
B07D (2x)	ARX1-
B07D (2x)	ARX1+
B07D (2x)	ARX2-
B07D (2x)	ARX2+
B07D (2x)	ARXC-
B07D (2x)	ARXC+
B07D (3x)	ARX-DDC-SCL
B07D (3x)	ARX-DDC-SDA
B07D (2x)	ARX-HOTPLUG
B06E (1x)	ASDO
B06G (1x)	ASDO
B04M (1x)	A-STBY
B10 (2x)	A-STBY
B04I (1x)	AUDIO-CL-L
B08A (1x)	AUDIO-CL-L
B04I (1x)	AUDIO-CL-R
B08A (1x)	AUDIO-CL-R
B04M (1x)	AUDIO-HDPH-L-AP
B08C (1x)	AUDIO-HDPH-L-AP
B04M (1x)	AUDIO-HDPH-R-AP
B08C (1x)	AUDIO-HDPH-R-AP
B04L (1x)	AUDIO-IN1-L
B08D (2x)	AUDIO-IN1-L
B04L (1x)	AUDIO-IN1-R
B08D (2x)	AUDIO-IN1-R
B04L (1x)	AUDIO-IN2-L
B08A (1x)	AUDIO-IN2-L
B04L (1x)	AUDIO-IN2-R
B08A (1x)	AUDIO-IN2-R
B04L (1x)	AUDIO-IN3-L
B08B (1x)	AUDIO-IN3-L
B04L (1x)	AUDIO-IN3-R
B08B (1x)	AUDIO-IN3-R
B04L (1x)	AUDIO-IN4-L
B07B (1x)	AUDIO-IN4-L
B04L (1x)	AUDIO-IN4-R
B07B (1x)	AUDIO-IN4-R
B04L (1x)	AUDIO-IN5-L
B08C (2x)	AUDIO-IN5-L
B04L (1x)	AUDIO-IN5-R
B08C (2x)	AUDIO-IN5-R
B04A (2x)	AUDIO-MUTE
B10 (1x)	AUDIO-MUTE
B04I (1x)	AUDIO-OUT-L
B08B (1x)	AUDIO-OUT-L
B04I (1x)	AUDIO-OUT-R
B08B (1x)	AUDIO-OUT-R
B04I (1x)	-AUDIO-R
B10 (1x)	-AUDIO-R
B04I (7x)	AUDIO-VDD
B04M (2x)	AUDIO-VDD
B08A (1x)	AV1-AUDIO-L
B08D (3x)	AV1-AUDIO-L
B08A (1x)	AV1-AUDIO-R
B08D (3x)	AV1-AUDIO-R
B08A (1x)	AV1-B
B08D (3x)	AV1-B
B04A (1x)	AV1-BLK
B08A (1x)	AV1-BLK
B08D (1x)	AV1-BLK
B08A (1x)	AV1-BLK-BO
B08D (1x)	AV1-BLK-BO
B08A (1x)	AV1-CVBS
B08D (3x)	AV1-CVBS
B08A (1x)	AV1-G
B08D (3x)	AV1-G
B04K (1x)	AV1-PB
B08D (2x)	AV1-PB
B04K (1x)	AV1-PR
B08D (2x)	AV1-PR
B08A (1x)	AV1-R
B08D (3x)	AV1-R
B04A (1x)	AV1-STATUS
B08A (1x)	AV1-STATUS
B04A (1x)	AV1-Y
B08D (2x)	AV1-Y
B04K (1x)	AV1-Y_CVBS
B08B (1x)	AV1-Y_CVBS
B08D (2x)	AV1-Y_CVBS
B04A (1x)	AV2-BLK
B08A (1x)	AV2-BLK
B04A (1x)	AV2-STATUS
B08A (1x)	AV2-STATUS
B04K (1x)	AV2-Y_CVBS
B08A (1x)	AV2-Y_CVBS
B08B (1x)	AV2-Y_CVBS
B04K (1x)	AV3-PB
B08A (1x)	AV3-PB
B04K (1x)	AV3-PR
B08A (1x)	AV3-PR
B04K (1x)	AV3-Y
B08A (1x)	AV3-Y
B04K (1x)	AV4-PB
B08A (1x)	AV4-PB
B04K (1x)	AV4-PR
B08A (1x)	AV4-PR
B04K (2x)	AV4-Y
B08A (1x)	AV4-Y
B08B (1x)	AV4-Y
B04K (1x)	AV5-PB
B08A (1x)	AV5-PB
B04K (1x)	AV5-PR
B08A (1x)	AV5-PR
B04K (2x)	AV5-Y
B08A (1x)	AV5-Y
B01B (1x)	BACKLIGHT-BOOST
B05H (1x)	BACKLIGHT-BOOST
B05H (1x)	BACKLIGHT-CONTROL-FPGA-IN
B06A (1x)	BACKLIGHT-CONTROL-FPGA-IN
B06G (1x)	BACKLIGHT-CONTROL-FPGA-IN
B05H (3x)	BACKLIGHT-CTRL
B01B (1x)	BACKLIGHT-OUT
B05E (1x)	BACKLIGHT-OUT
B05H (1x)	BACKLIGHT-OUT
B06G (1x)	BACKLIGHT-OUT
B05H (1x)	BACKLIGHT-OUT2
B06G (1x)	BACKLIGHT-OUT2
B01B (1x)	BACKLIGHT-PWM-ANA-DISP
B05H (1x)	BACKLIGHT-PWM-ANA-DISP
B05H (2x)	BACKLIGHT-PWM-ANA-SSB
B02A (3x)	B-IF-_N-IF-
B02A (3x)	B-IF+_N-IF+
B07D (4x)	BIN-5V
B06A (2x)	BL-CLK
B06A (2x)	BL-CS
B06A (2x)	BL-HS
B06A (2x)	BL-MISO
B06A (2x)	BL-MOSI
B05D (1x)	BL-OSCLK
B06A (1x)	BL-OSCLK
B05D (1x)	BL-SCK
B06A (1x)	BL-SCK
B05D (1x)	BL-SD0
B06A (1x)	BL-SD0
B06A (2x)	BL-VS
B05D (1x)	BL-WS
B06A (1x)	BL-WS
B08D (2x)	BO-AUDIO-L
B08D (2x)	BO-AUDIO-R
B08D (2x)	BO-B
B08D (2x)	BO-CVBS
B08D (2x)	BO-G
B04A (2x)	BOLT-ON-IO
B04N (1x)	BOLT-ON-IO
B08D (3x)	BOLT-ON-IO
B04A (2x)	BOLT-ON-TS-ENn
B04N (1x)	BOLT-ON-TS-ENn
B05H (3x)	BOOST-CTRL
B04E (2x)	BOOTMODE
B08D (2x)	BO-R
B07D (2x)	BRX0-
B07D (2x)	BRX0+
B07D (2x)	BRX1-
B07D (2x)	BRX1+
B07D (2x)	BRX2-
B07D (2x)	BRX2+
B07D (2x)	BRXC-
B07D (2x)	BRXC+
B07D (3x)	BRX-DDC-SCL
B07D (3x)	BRX-DDC-SDA
B07D (2x)	BRX-HOTPLUG
B04K (1x)	B-VGA
B08B (1x)	B-VGA
B04N (1x)	CA-ADDEN
B07H (3x)	CA-ADDEN
B04N (1x)	CA-CD1
B07A (2x)	CA-CD1
B04N (1x)	CA-CD2
B07A (2x)	CA-CD2
B07A (1x)	CA-CE1
B07H (1x)	CA-CE1
B07A (1x)	CA-CE2
B07H (1x)	CA-CE2
B04N (1x)	CA-DATADIR
B07H (1x)	CA-DATADIR
B04N (1x)	CA-DATAEN
B07H (1x)	CA-DATAEN
B07A (2x)	CA-INPACK
B07A (1x)	CA-IORD
B07H (1x)	CA-IORD
B07A (1x)	CA-IOWR
B07H (1x)	CA-IOWR
B04N (1x)	CA-MDI0
B07A (1x)	CA-MDI0
B04N (1x)	CA-MDI1
B07A (1x)	CA-MDI1
B04N (1x)	CA-MDI2
B07A (1x)	CA-MDI2
B04N (1x)	CA-MDI3
B07A (1x)	CA-MDI3
B04N (1x)	CA-MDI4
B07A (1x)	CA-MDI4
B04N (1x)	CA-MDI5
B07A (1x)	CA-MDI5
B04N (1x)	CA-MDI6
B07A (1x)	CA-MDI6
B04N (1x)	CA-MDI7
B07A (1x)	CA-MDI7
B04N (1x)	CA-MDO0
B07A (2x)	CA-MDO0
B04N (1x)	CA-MDO1
B07A (2x)	CA-MDO1
B04N (1x)	CA-MDO2
B07A (2x)	CA-MDO2
B04N (1x)	CA-MDO3
B07A (2x)	CA-MDO3
B04N (1x)	CA-MDO4
B07A (2x)	CA-MDO4
B04N (1x)	CA-MDO5
B07A (2x)	CA-MDO5
B04N (1x)	CA-MDO6
B07A (2x)	CA-MDO6
B04N (1x)	CA-MDO7
B07A (2x)	CA-MDO7
B04N (1x)	CA-MICLK
B07A (1x)	CA-MICLK
B04N (1x)	CA-MISTRT
B07A (1x)	CA-MISTRT
B04N (1x)	CA-MIVAL
B07A (1x)	CA-MIVAL
B04N (2x)	CA-MOCLK_VS2
B07A (2x)	CA-MOCLK_VS2
B04N (1x)	CA-MOSTRT
B07A (2x)	CA-MOSTRT
B04N (1x)	CA-MOVAL
B07A (2x)	CA-MOVAL
B07A (1x)	CA-OE
B07H (1x)	CA-OE
B07A (1x)	CA-REG
B07H (1x)	CA-REG
B04N (1x)	CA-RST
B07A (2x)	CA-RST
B04N (1x)	CA-VS1
B07A (2x)	CA-VS1
B07A (2x)	CA-WAIT
B07H (1x)	CA-WAIT
B07A (1x)	CA-WE
B07H (1x)	CA-WE
B06A (3x)	CCLK
B04A (2x)	CEC-HDMI
B07D (1x)	CEC-HDMI
B07D (4x)	CIN-5V
B06G (2x)	CLK-OUT2-PNX5100
B05F (1x)	CLK-OUT-PNX5100
B06A (1x)	CLK-OUT-PNX5100
B06G (1x)	CLK-OUT-PNX5100
B06E (1x)	CON20
B06G (1x)	CON20
B06E (1x)	CON21
B06G (1x)	CON21
B06E (1x)	CON22
B06G (1x)	CON22
B06E (1x)	CON23
B06G (1x)	CON23
B06E (1x)	CON26
B06G (1x)	CON26
B06E (1x)	CON27
B06G (1x)	CON27
B06E (1x)	CONF-DONE
B06G (1x)	CONF-DONE
B07D (2x)	CRX0-
B07D (2x)	CRX0+
B07D (2x)	CRX1-
B07D (2x)	CRX1+
B07D (2x)	CRX2-
B07D (2x)	CRX2+
B07D (2x)	CRXC-
B07D (2x)	CRXC+
B07D (3x)	CRX-DDC-SCL
B07D (3x)	CRX-DDC-SDA
B07D (2x)	CRX-HOTPLUG
B06A (4x)	CSO-B
B05H (2x)	CTRL1-PNX5100
B05H (2x)	CTRL2-PNX5100
B05H (2x)	CTRL3-PNX5100
B05H (3x)	CTRL4-PNX5100
B05E (1x)	CTRL-DISP1
B05H (1x)	CTRL-DISP1
B05E (1x)	CTRL-DISP2
B05H (1x)	CTRL-DISP2
B05E (1x)	CTRL-DISP3
B05H (1x)	CTRL-DISP3
B05E (1x)	CTRL-DISP4
B05H (2x)	CTRL-DISP4
B02B (1x)	CVBS4
B04K (1x)	CVBS4
B08B (2x)	CVBS-MON-OUT-CINCH
B08A (2x)	CVBS-OUT-SC1
B02B (1x)	CVBS-TER-OUT
B08A (1x)	CVBS-TER-OUT
B08D (1x)	CVBS-TER-OUT
B06E (1x)	DATA0
B06G (1x)	DATA0
B06E (1x)	DCLK
B06G (1x)	DCLK
B04H (1x)	DDCA-SCL
B07E (1x)	DDCA-SCL
B04H (1x)	DDCA-SDA
B07E (1x)	DDCA-SDA
B04H (1x)	DDC-SCL
B07D (1x)	DDC-SCL
B04H (1x)	DDC-SDA
B07D (1x)	DDC-SDA
B04G (3x)	DDR2-A0
B04G (3x)	DDR2-A1
B04G (3x)	DDR2-A10
B04G (3x)	DDR2-A11
B04G (3x)	DDR2-A12
B04G (3x)	DDR2-A2
B04G (3x)	DDR2-A3
B04G (3x)	DDR2-A4
B04G (3x)	DDR2-A5
B04G (3x)	DDR2-A6
B04G (3x)	DDR2-A7
B04G (3x)	DDR2-A8
B04G (3x)	DDR2-A9
B04G (3x)	DDR2-BA0
B04G (3x)	DDR2-BA1
B04G (3x)	DDR2-BA2
B04G (3x)	DDR2-CAS
B04G (3x)	DDR2-CKE
B04G (4x)	DDR2-CLK_N
B04G (4x)	DDR2-CLK_P
B04G (3x)	DDR2-CS
B04G (2x)	DDR2-D0
B04G (2x)	DDR2-D1
B04G (2x)	DDR2-D10
B04G (2x)	DDR2-D11
B04G (2x)	DDR2-D12
B04G (2x)	DDR2-D13
B04G (2x)	DDR2-D14
B04G (2x)	DDR2-D15
B04G (2x)	DDR2-D16
B04G (2x)	DDR2-D17
B04G (2x)	DDR2-D18
B04G (2x)	DDR2-D19
B04G (2x)	DDR2-D2
B04G (2x)	DDR2-D20
B04G (2x)	DDR2-D21
B04G (2x)	DDR2-D22
B04G (2x)	DDR2-D23
B04G (2x)	DDR2-D24
B04G (2x)	DDR2-D25
B04G (2x)	DDR2-D26
B04G (2x)	DDR2-D27
B04G (2x)	DDR2-D28
B04G (2x)	DDR2-D29
B04G (2x)	DDR2-D3
B04G (2x)	DDR2-D30
B04G (2x)	DDR2-D31
B04G (2x)	DDR2-D4
B04G (2x)	DDR2-D5
B04G (2x)	DDR2-D6
B04G (2x)	DDR2-D7
B04G (2x)	DDR2-D8
B04G (2x)	DDR2-D9
B04G (2x)	DDR2-DQM0
B04G (2x)	DDR2-DQM1
B04G (2x)	DDR2-DQM2
B04G (2x)	DDR2-DQM3
B04G (2x)	DDR2-DQS0_N
B04G (2x)	DDR2-DQS0_P
B04G (2x)	DDR2-DQS1_N
B04G (2x)	DDR2-DQS1_P
B04G (2x)	DDR2-DQS2_N
B04G (2x)	DDR2-DQS2_P
B04G (2x)	DDR2-DQS3_N
B04G (2x)	DDR2-DQS3_P
B04G (3x)	DDR2-ODT
B04G (3x)	DDR2-RAS
B04G (2x)	DDR2-VREF-CTRL
B04G (3x)	DDR2-VREF-DDR
B04G (3x)	DDR2-WE
B04A (3x)	DETECT1
B01B (1x)	DETECT-12V
B04A (1x)	DETECT-12V
B04A (3x)	DETECT2
B07D (4x)	DIN-5V
B06A (2x)	DONE
B06F (2x)	DQ1(0)
B06F (2x)	DQ1(1)
B06F (2x)	DQ1(10)
B06F (2x)	DQ1(11)
B06F (2x)	DQ1(12)
B06F (2x)	DQ1(13)
B06F (2x)	DQ1(14)
B06F (2x)	DQ1(15)
B06F (2x)	DQ1(2)
B06F (2x)	DQ1(3)
B06F (2x)	DQ1(4)
B06F (2x)	DQ1(5)
B06F (2x)	DQ1(6)
B06F (2x)	DQ1(7)
B06F (2x)	DQ1(8)
B06F (2x)	DQ1(9)
B06F (2x)	DQS10
B06F (2x)	DQS11
B07D (2x)	DRX0-
B07D (2x)	DRX0+
B07D (2x)	DRX1-
B07D (2x)	DRX1+
B07D (2x)	DRX2-
B07D (2x)	DRX2+
B07D (2x)	DRXC-
B07D (2x)	DRXC+
B07D (3x)	DRX-DDC-SCL
B07D (3x)	DRX-DDC-SDA
B07D (2x)	DRX-HOTPLUG
B04A (2x)	EA
B07E (4x)	EIN-5V
B04A (2x)	EJTAG-DETECT
B06B (1x)	EJTAG-DETECT
B05F (1x)	EJTAG-PNX5100-TCK
B05F (1x)	EJTAG-PNX5100-TDI
B05F (1x)	EJTAG-PNX5100-TDO
B05F (1x)	EJTAG-PNX5100-TMS
B05F (1x)	EJTAG-PNX5100-TRSTn
B04E (2x)	EJTAG-TCK
B06B (1x)	EJTAG-TCK
B04E (2x)	EJTAG-TDI
B06B (1x)	EJTAG-TDI
B04E (2x)	EJTAG-TDO
B06B (1x)	EJTAG-TDO
B04E (2x)	EJTAG-TMS
B06B (1x)	EJTAG-TMS
B04E (2x)	EJTAG-TRSTN
B06B (1x)	EJTAG-TRSTN
B01B (1x)	ENABLE-3V3
B04A (2x)	ENABLE-3V3
B01A (1x)	ENABLE-3V3-5V
B01B (1x)	ENABLE-3V3-5V
B01C (1x)	ENABLE-3V3-5V
B07E (3x)	ERX-DDC-SCL
B07E (3x)	ERX-DDC-SDA
B07E (3x)	ERX-HOTPLUG
B06C (2x)	FAN1-DRV
B06C (2x)	FAN1-OUT
B06C (2x)	FAN2-DRV
B05H (1x)	FAN-CTRL-1
B06C (1x)	FAN-CTRL-1
B05H (1x)	FAN-CTRL-2
B02B (1x)	FE-CLK
B04N (3x)	FE-CLK
B02B (1x)	FE-DATA0
B04N (3x)	FE-DATA0
B02B (1x)	FE-DATA1
B04N (3x)	FE-DATA1
B02B (1x)	FE-DATA2
B04N (3x)	FE-DATA2
B02B (1x)	FE-DATA3
B04N (3x)	FE-DATA3
B02B (1x)	FE-DATA4
B04N (3x)	FE-DATA4
B02B (1x)	FE-DATA5
B04N (3x)	FE-DATA5
B02B (1x)	FE-DATA6
B04N (3x)	FE-DATA6
B02B (1x)	FE-DATA7
B04N (3x)	FE-DATA7
B04N (4x)	FE-ERR
B02B (1x)	FE-SOP
B04N (3x)	FE-SOP
B02B (1x)	FE-VALID
B04N (3x)	FE-VALID
B04K (1x)	FRONT-C
B08C (2x)	FRONT-C
B04K (1x)	FRONT-Y_CVBS
B08C (2x)	FRONT-Y_CVBS
B10 (2x)	GND-A
B01B (1x)	GND-AUDIO
B10 (16x)	GND-AUDIO
B01A (15x)	GND-SIG
B01C (15x)	GND-SIG1
B04K (1x)	G-VGA
B08B (1x)	G-VGA
B04H (1x)	HDMIA-RX0-
B07E (2x)	HDMIA-RX0-
B04H (1x)	HDMIA-RX0+
B07E (2x)	HDMIA-RX0+
B04H (1x)	HDMIA-RX1-
B07E (2x)	HDMIA-RX1-
B04H (1x)	HDMIA-RX1+
B07E (2x)	HDMIA-RX1+
B04H (1x)	HDMIA-RX2-
B07E (2x)	HDMIA-RX2-
B04H (1x)	HDMIA-RX2+
B07E (2x)	HDMIA-RX2+
B04H (1x)	HDMIA-RXC-
B07E (2x)	HDMIA-RXC-
B04H (1x)	HDMIA-RXC+
B07E (2x)	HDMIA-RXC+
B04H (1x)	HDMIB-RX0-
B07D (1x)	HDMIB-RX0-
B04H (1x)	HDMIB-RX0+
B07D (1x)	HDMIB-RX0+
B04H (1x)	HDMIB-RX1-
B07D (1x)	HDMIB-RX1-
B04H (1x)	HDMIB-RX1+
B07D (1x)	HDMIB-RX1+
B04H (1x)	HDMIB-RX2-
B07D (1x)	HDMIB-RX2-
B04H (1x)	HDMIB-RX2+
B07D (1x)	HDMIB-RX2+
B04H (1x)	HDMIB-RXC-
B07D (1x)	HDMIB-RXC-
B04H (1x)	HDMIB-RXC+
B07D (1x)	HDMIB-RXC+
B04H (1x)	HOT-PLUG
B04H (1x)	HOT-PLUG-A
B07E (1x)	HOT-PLUG-A
B04K (1x)	H-SYNC-VGA
B08B (1x)	H-SYNC-VGA
B04N (1x)	I2C-SCL
B07F (1x)	I2C-SCL
B04N (1x)	I2C-SDA
B07F (1x)	I2C-SDA
B09A (2x)	IDSEL
B02A (1x)	IF-
B02B (1x)	IF-
B02A (1x)	IF+
B02B (1x)	IF+
B02A (2x)	IF-AGC
B02B (1x)	IF-AGC
B04K (1x)	IF-N
B02B (1x)	IF-P
B04K (1x)	IF-P
B09A (1x)	IRQA-mPCI
B09A (1x)	IRQB-mPCI
B04E (2x)	IRQ-CA
B04N (1x)	IRQ-CA
B07A (2x)	IRQ-CA
B04E (2x)	IRQ-PCI
B07G (1x)	IRQ-PCI
B09A (2x)	IRQ-PCI
B01B (1x)	KEYBOARD
B04A (2x)	KEYBOARD
B09B (1x)	KEYBOARD
B04A (3x)	LAMP-ON
B01B (1x)	LAMP-ON-OUT
B04A (1x)	LAMP-ON-OUT
B05E (1x)	LAMP-ON-OUT
B05H (2x)	LCD-PWR-ON
B01B (2x)	LED1
B04A (2x)	LED1
B01B (2x)	LED2
B04A (2x)	LED2
B10 (3x)	LEFT-SPEAKER
B01B (2x)	LIGHT-SENSOR
B04A (1x)	LIGHT-SENSOR
B09A (2x)	M66EN
B07A (4x)	MDO0
B07A (4x)	MDO1
B07A (4x)	MDO2
B07A (4x)	MDO3
B07A (4x)	MDO4
B07A (4x)	MDO5
B07A (4x)	MDO6
B07A (4x)	MDO7
B04A (2x)	MHP-SWITCH
B08D (3x)	MHP-SWITCH
B06A (3x)	MISO
B06F (1x)	MM1-A0
B06G (1x)	MM1-A0
B06F (1x)	MM1-A1
B06G (1x)	MM1-A1
B06F (1x)	MM1-A10
B06G (1x)	MM1-A10
B06F (1x)	MM1-A11
B06G (1x)	MM1-A11
B06F (1x)	MM1-A12
B06G (1x)	MM1-A12
B06F (1x)	MM1-A2
B06G (1x)	MM1-A2
B06F (1x)	MM1-A3
B06G (1x)	MM1-A3
B06F (1x)	MM1-A4
B06G (1x)	MM1-A4
B06F (1x)	MM1-A5
B06G (1x)	MM1-A5
B06F (1x)	MM1-A6
B06G (1x)	MM1-A6
B06F (1x)	MM1-A7
B06G (1x)	MM1-A7
B06F (1x)	MM1-A8
B06G (1x)	MM1-A8
B06F (1x)	MM1-A9
B06G (1x)	MM1-A9
B06F (1x)	MM1-BA0
B06G (1x)	MM1-BA0
B06F (1x)	MM1-BA1
B06G (1x)	MM1-BA1
B06F (1x)	MM1-CAS
B06G (1x)	MM1-CAS
B06F (1x)	MM1-CKE
B06G (1x)	MM1-CKE
B06F (1x)	MM1-CLK-
B06G (1x)	MM1-CLK-
B06F (1x)	MM1-CLK+
B06G (1x)	MM1-CLK+
B06F (1x)	MM1-CS0
B06G (1x)	MM1-CS0
B06F (1x)	MM1-D0
B06G (1x)	MM1-D0
B06F (1x)	MM1-D1
B06G (1x)	MM1-D1
B06F (1x)	MM1-D10
B06G (1x)	MM1-D10
B06F (1x)	MM1-D11
B06G (1x)	MM1-D11
B06F (1x)	MM1-D12
B06G (1x)	MM1-D12
B06F (1x)	MM1-D13
B06G (1x)	MM1-D13
B06F (1x)	MM1-D14
B06G (1x)	MM1-D14
B06F (1x)	MM1-D15
B06G (1x)	MM1-D15
B06F (1x)	MM1-D2
B06G (1x)	MM1-D2
B06F (1x)	MM1-D3
B06G (1x)	MM1-D3
B06F (1x)	MM1-D4
B06G (1x)	MM1-D4
B06F (1x)	MM1-D5
B06G (1x)	MM1-D5
B06F (1x)	MM1-D6
B06G (1x)	MM1-D6
B06F (1x)	MM1-D7
B06G (1x)	MM1-D7
B06F (1x)	MM1-D8
B06G (1x)	MM1-D8
B06F (1x)	MM1-D9
B06G (1x)	MM1-D9
B06F (1x)	MM1-DQS0
B06G (1x)	MM1-DQS0
B06F (1x)	MM1-DQS1
B06G (1x)	MM1-DQS1
B06F (1x)	MM1-RAS
B06G (1x)	MM1-RAS

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SSB: SRP List Part 2

Netname	Schematic
B06F (1×)	MM1-WE
B06G (1×)	MM1-WE
B07A (4×)	MOCLK_VS2
B06A (3×)	MOSI
B07A (4×)	MOSTRT
B07A (4×)	MOVAL
B09A (2×)	MPCIACT
B06G (1×)	MSEL0
B06G (1×)	MSEL1
B06G (1×)	MSEL2
B06G (1×)	MSEL3
B07F (2×)	NAND-AD(0)
B07F (2×)	NAND-AD(1)
B07F (2×)	NAND-AD(2)
B07F (2×)	NAND-AD(3)
B07F (2×)	NAND-AD(4)
B07F (2×)	NAND-AD(5)
B07F (2×)	NAND-AD(6)
B07F (2×)	NAND-AD(7)
B07F (2×)	NAND-ALE
B07F (2×)	NAND-CLE
B07F (2×)	NAND-REn
B07F (2×)	NAND-WEn
B06G (2×)	nCE
B06G (2×)	nCONFIG
B06E (1×)	nCSO
B06G (1×)	nCSO
B06G (2×)	nSTATUS
B07D (6×)	PCEC-HDMI
B07E (2×)	PCEC-HDMI
B04F (1×)	PCI-AD0
B05G (1×)	PCI-AD0
B07F (1×)	PCI-AD0
B07G (1×)	PCI-AD0
B07H (1×)	PCI-AD0
B09A (1×)	PCI-AD0
B04F (1×)	PCI-AD1
B05G (1×)	PCI-AD1
B07F (1×)	PCI-AD1
B07G (1×)	PCI-AD1
B07H (2×)	PCI-AD1
B09A (1×)	PCI-AD1
B04F (1×)	PCI-AD10
B05G (1×)	PCI-AD10
B07G (1×)	PCI-AD10
B07H (1×)	PCI-AD10
B09A (1×)	PCI-AD10
B04F (1×)	PCI-AD11
B05G (1×)	PCI-AD11
B07G (1×)	PCI-AD11
B07H (1×)	PCI-AD11
B09A (2×)	PCI-AD11
B04F (1×)	PCI-AD12
B05G (1×)	PCI-AD12
B07G (1×)	PCI-AD12
B07H (1×)	PCI-AD12
B09A (2×)	PCI-AD12
B04F (1×)	PCI-AD13
B05G (1×)	PCI-AD13
B07G (1×)	PCI-AD13
B07H (1×)	PCI-AD13
B09A (2×)	PCI-AD13
B04F (1×)	PCI-AD14
B05G (1×)	PCI-AD14
B07G (1×)	PCI-AD14
B07H (1×)	PCI-AD14
B09A (1×)	PCI-AD14
B04F (1×)	PCI-AD15
B05G (1×)	PCI-AD15
B07G (1×)	PCI-AD15
B09A (1×)	PCI-AD15
B04F (1×)	PCI-AD16
B05G (1×)	PCI-AD16
B07G (1×)	PCI-AD16
B07H (1×)	PCI-AD16
B09A (1×)	PCI-AD16
B04F (1×)	PCI-AD17
B05G (1×)	PCI-AD17
B07G (1×)	PCI-AD17
B07H (1×)	PCI-AD17
B09A (1×)	PCI-AD17
B04F (1×)	PCI-AD18
B05G (1×)	PCI-AD18
B07G (1×)	PCI-AD18
B07H (1×)	PCI-AD18
B09A (1×)	PCI-AD18
B04F (1×)	PCI-AD19
B05G (1×)	PCI-AD19
B07G (1×)	PCI-AD19
B07H (1×)	PCI-AD19
B09A (1×)	PCI-AD19
B04F (1×)	PCI-AD2
B05G (1×)	PCI-AD2
B07G (1×)	PCI-AD2
B07H (1×)	PCI-AD2
B09A (1×)	PCI-AD2
B04F (1×)	PCI-AD20
B05G (1×)	PCI-AD20
B07G (1×)	PCI-AD20
B09A (1×)	PCI-AD20
B04F (1×)	PCI-AD21
B05G (1×)	PCI-AD21
B07G (1×)	PCI-AD21
B09A (1×)	PCI-AD21
B04F (1×)	PCI-AD22
B05G (1×)	PCI-AD22
B07G (1×)	PCI-AD22
B07H (1×)	PCI-AD22
B09A (1×)	PCI-AD22
B04F (1×)	PCI-AD23
B05G (1×)	PCI-AD23
B07G (2×)	PCI-AD23
B07H (1×)	PCI-AD23
B09A (1×)	PCI-AD23
B04F (2×)	PCI-AD24
B05G (1×)	PCI-AD24
B07F (1×)	PCI-AD24
B07G (1×)	PCI-AD24
B07H (1×)	PCI-AD24
B09A (1×)	PCI-AD24
B04F (1×)	PCI-AD25
B05G (2×)	PCI-AD25
B07F (1×)	PCI-AD25
B07G (1×)	PCI-AD25
B07H (1×)	PCI-AD25
B09A (1×)	PCI-AD25
B04F (1×)	PCI-AD26
B05G (1×)	PCI-AD26
B07F (1×)	PCI-AD26
B07G (1×)	PCI-AD26
B07H (1×)	PCI-AD26
B09A (1×)	PCI-AD26
B04F (1×)	PCI-AD27
B05G (1×)	PCI-AD27
B07F (1×)	PCI-AD27
B07G (1×)	PCI-AD27
B07H (1×)	PCI-AD27
B09A (1×)	PCI-AD27
B04F (1×)	PCI-AD28
B05G (1×)	PCI-AD28
B07F (1×)	PCI-AD28
B07G (1×)	PCI-AD28
B07H (1×)	PCI-AD28
B09A (1×)	PCI-AD28
B04F (1×)	PCI-AD29
B05G (1×)	PCI-AD29
B07F (1×)	PCI-AD29
B07G (1×)	PCI-AD29
B07H (1×)	PCI-AD29
B09A (1×)	PCI-AD29
B04F (1×)	PCI-AD3
B05G (1×)	PCI-AD3
B07G (1×)	PCI-AD3
B07H (1×)	PCI-AD3
B09A (1×)	PCI-AD3
B04F (1×)	PCI-AD30
B05G (1×)	PCI-AD30
B07F (1×)	PCI-AD30
B07G (1×)	PCI-AD30
B07H (1×)	PCI-AD30
B09A (1×)	PCI-AD30
B04F (1×)	PCI-AD31
B05G (1×)	PCI-AD31
B07F (1×)	PCI-AD31
B07G (1×)	PCI-AD31
B07H (1×)	PCI-AD31
B09A (1×)	PCI-AD31
B04F (1×)	PCI-AD4
B05G (1×)	PCI-AD4
B07G (1×)	PCI-AD4
B07H (1×)	PCI-AD4
B09A (1×)	PCI-AD4
B04F (1×)	PCI-AD5
B05G (1×)	PCI-AD5
B07G (1×)	PCI-AD5
B07H (1×)	PCI-AD5
B09A (1×)	PCI-AD5
B04F (1×)	PCI-AD6
B05G (1×)	PCI-AD6
B07G (1×)	PCI-AD6
B07H (1×)	PCI-AD6
B09A (1×)	PCI-AD6
B04F (1×)	PCI-AD7
B05G (1×)	PCI-AD7
B07G (1×)	PCI-AD7
B07H (1×)	PCI-AD7
B09A (1×)	PCI-AD7
B04F (1×)	PCI-AD8
B05G (1×)	PCI-AD8
B07G (1×)	PCI-AD8
B07H (1×)	PCI-AD8
B09A (1×)	PCI-AD8
B04F (1×)	PCI-AD9
B05G (1×)	PCI-AD9
B07G (1×)	PCI-AD9
B07H (1×)	PCI-AD9
B09A (1×)	PCI-AD9
B04F (1×)	PCI-CBE0
B05G (1×)	PCI-CBE0
B07G (1×)	PCI-CBE0
B09A (1×)	PCI-CBE0
B04F (1×)	PCI-CBE1
B05G (1×)	PCI-CBE1
B07F (1×)	PCI-CBE1
B07G (1×)	PCI-CBE1
B07H (1×)	PCI-CBE1
B09A (1×)	PCI-CBE1
B04F (1×)	PCI-CBE2
B05G (1×)	PCI-CBE2
B07F (1×)	PCI-CBE2
B07G (1×)	PCI-CBE2
B07H (1×)	PCI-CBE2
B09A (1×)	PCI-CBE2
B04F (1×)	PCI-CBE3
B05G (1×)	PCI-CBE3
B07G (1×)	PCI-CBE3
B09A (1×)	PCI-CBE3
B04F (2×)	PCI-CLK-ETHERNET
B07G (1×)	PCI-CLK-ETHERNET
B04F (2×)	PCI-CLK-MINI
B09A (1×)	PCI-CLK-MINI
B04E (1×)	PCI-CLK-OUT
B04F (3×)	PCI-CLK-OUT
B04F (2×)	PCI-CLK-PNX5100
B05G (1×)	PCI-CLK-PNX5100
B04F (3×)	PCI-CLK-PNX8535
B09A (2×)	PCI-CLKRUN
B04F (2×)	PCI-DEVSEL
B05G (1×)	PCI-DEVSEL
B07G (1×)	PCI-DEVSEL
B09A (1×)	PCI-DEVSEL
B04F (2×)	PCI-FRAME
B05G (1×)	PCI-FRAME
B07G (1×)	PCI-FRAME
B09A (1×)	PCI-FRAME
B04F (2×)	PCI-GNT
B04F (2×)	PCI-GNT-B
B04F (1×)	PCI-GNT-ETH
B07G (1×)	PCI-GNT-ETH
B04F (1×)	PCI-GNT-MINI
B09A (1×)	PCI-GNT-MINI
B04F (2×)	PCI-IRDY
B05G (1×)	PCI-IRDY
B07G (1×)	PCI-IRDY
B09A (1×)	PCI-IRDY
B04F (1×)	PCI-PAR
B05G (1×)	PCI-PAR
B07G (1×)	PCI-PAR
B09A (1×)	PCI-PAR
B04F (2×)	PCI-PERR
B05G (1×)	PCI-PERR
B07G (1×)	PCI-PERR
B09A (1×)	PCI-PERR
B04F (2×)	PCI-REQ
B04F (2×)	PCI-REQ-B
B04F (1×)	PCI-REQ-ETH
B07G (1×)	PCI-REQ-ETH
B04F (1×)	PCI-REQ-MINI
B09A (1×)	PCI-REQ-MINI
B04F (2×)	PCI-SERR
B05G (1×)	PCI-SERR
B07G (1×)	PCI-SERR
B09A (1×)	PCI-SERR
B04F (2×)	PCI-STOP
B05G (1×)	PCI-STOP
B07G (1×)	PCI-STOP
B09A (1×)	PCI-STOP
B04F (2×)	PCI-TRDY
B05G (1×)	PCI-TRDY
B07G (1×)	PCI-TRDY
B09A (1×)	PCI-TRDY
B07A (1×)	PCMCIA-A0
B07H (1×)	PCMCIA-A0
B07A (1×)	PCMCIA-A1
B07H (1×)	PCMCIA-A1
B07A (1×)	PCMCIA-A10
B07H (1×)	PCMCIA-A10
B07A (1×)	PCMCIA-A11
B07H (1×)	PCMCIA-A11
B07A (1×)	PCMCIA-A12
B07H (1×)	PCMCIA-A12
B07A (1×)	PCMCIA-A13
B07H (1×)	PCMCIA-A13
B07A (1×)	PCMCIA-A14
B07H (1×)	PCMCIA-A14
B07A (1×)	PCMCIA-A2
B07H (1×)	PCMCIA-A2
B07A (1×)	PCMCIA-A3
B07H (1×)	PCMCIA-A3
B07A (1×)	PCMCIA-A4
B07H (1×)	PCMCIA-A4
B07A (1×)	PCMCIA-A5
B07H (1×)	PCMCIA-A5
B07A (1×)	PCMCIA-A6
B07H (1×)	PCMCIA-A6
B07A (1×)	PCMCIA-A7
B07H (1×)	PCMCIA-A7
B07A (1×)	PCMCIA-A8
B07H (1×)	PCMCIA-A8
B07A (1×)	PCMCIA-A9
B07H (1×)	PCMCIA-A9
B07A (1×)	PCMCIA-D0
B07H (1×)	PCMCIA-D0
B07A (1×)	PCMCIA-D1
B07H (1×)	PCMCIA-D1
B07A (1×)	PCMCIA-D2
B07H (1×)	PCMCIA-D2
B07A (1×)	PCMCIA-D3
B07H (1×)	PCMCIA-D3
B07A (1×)	PCMCIA-D4
B07H (1×)	PCMCIA-D4
B07A (1×)	PCMCIA-D5
B07H (1×)	PCMCIA-D5
B07A (1×)	PCMCIA-D6
B07H (1×)	PCMCIA-D6
B07A (1×)	PCMCIA-D7
B07H (1×)	PCMCIA-D7
B07A (5×)	PCMCIA-VCC-VPP
B02A (2×)	PDN
B02B (1×)	PDN
B02A (1×)	PDP
B02B (1×)	PDP
B09A (2×)	PME
B05A (3×)	PNX5100-DDR2-A0
B05A (3×)	PNX5100-DDR2-A1
B05A (3×)	PNX5100-DDR2-A10
B05A (3×)	PNX5100-DDR2-A11
B05A (3×)	PNX5100-DDR2-A12
B05A (3×)	PNX5100-DDR2-A2
B05A (3×)	PNX5100-DDR2-A3
B05A (3×)	PNX5100-DDR2-A4
B05A (3×)	PNX5100-DDR2-A5
B05A (3×)	PNX5100-DDR2-A6
B05A (3×)	PNX5100-DDR2-A7
B05A (3×)	PNX5100-DDR2-A8
B05A (3×)	PNX5100-DDR2-A9
B05A (3×)	PNX5100-DDR2-BA0
B05A (3×)	PNX5100-DDR2-BA1
B05A (3×)	PNX5100-DDR2-CAS
B05A (3×)	PNX5100-DDR2-CKE
B05A (3×)	PNX5100-DDR2-CLK_N
B05A (3×)	PNX5100-DDR2-CLK_P
B05A (3×)	PNX5100-DDR2-CS
B05A (2×)	PNX5100-DDR2-D0
B05A (2×)	PNX5100-DDR2-D1
B05A (2×)	PNX5100-DDR2-D10
B05A (2×)	PNX5100-DDR2-D11
B05A (2×)	PNX5100-DDR2-D12
B05A (2×)	PNX5100-DDR2-D13
B05A (2×)	PNX5100-DDR2-D14
B05A (2×)	PNX5100-DDR2-D15
B05A (2×)	PNX5100-DDR2-D16
B05A (2×)	PNX5100-DDR2-D17
B05A (2×)	PNX5100-DDR2-D18
B05A (2×)	PNX5100-DDR2-D19
B05A (2×)	PNX5100-DDR2-D2
B05A (2×)	PNX5100-DDR2-D20
B05A (2×)	PNX5100-DDR2-D21
B05A (2×)	PNX5100-DDR2-D22
B05A (2×)	PNX5100-DDR2-D23
B05A (2×)	PNX5100-DDR2-D24
B05A (2×)	PNX5100-DDR2-D25
B05A (2×)	PNX5100-DDR2-D26
B05A (2×)	PNX5100-DDR2-D27
B05A (2×)	PNX5100-DDR2-D28
B05A (2×)	PNX5100-DDR2-D29
B05A (2×)	PNX5100-DDR2-D3
B05A (2×)	PNX5100-DDR2-D30
B05A (2×)	PNX5100-DDR2-D31
B05A (2×)	PNX5100-DDR2-D4
B05A (2×)	PNX5100-DDR2-D5
B05A (2×)	PNX5100-DDR2-D6
B05A (2×)	PNX5100-DDR2-D7
B05A (2×)	PNX5100-DDR2-D8
B05A (2×)	PNX5100-DDR2-D9
B05A (2×)	PNX5100-DDR2-DQM0
B05A (2×)	PNX5100-DDR2-DQM1
B05A (2×)	PNX5100-DDR2-DQM2
B05A (2×)	PNX5100-DDR2-DQM3
B05A (2×)	PNX5100-DDR2-DQS0_N
B05A (2×)	PNX5100-DDR2-DQS0_P
B05A (2×)	PNX5100-DDR2-DQS1_N
B05A (2×)	PNX5100-DDR2-DQS1_P
B05A (2×)	PNX5100-DDR2-DQS2_N
B05A (2×)	PNX5100-DDR2-DQS2_P
B05A (2×)	PNX5100-DDR2-DQS3_N
B05A (2×)	PNX5100-DDR2-DQS3_P
B05A (3×)	PNX5100-DDR2-ODT
B05A (3×)	PNX5100-DDR2-RAS
B05A (2×)	PNX5100-DDR2-VREF-CTRL
B05A (3×)	PNX5100-DDR2-VREF-DDR
B05A (3×)	PNX5100-DDR2-WE
B05F (1×)	PNX5100-RST-OUT
B05I (1×)	PNX5100-RST-OUT
B01B (1×)	POWER-OK
B04A (2×)	POWER-OK
B06A (2×)	PROG-B
B04A (2×)	PSEN
B01B (1×)	RC
B04A (2×)	RC
B04A (1×)	RC-IN
B08C (1×)	RC-IN
B04A (1×)	RC-OUT
B08C (1×)	RC-OUT
B04A (4×)	RC-UP
B08D (1×)	RC-UP
B07D (2×)	REF-3V3
B04A (2×)	REGIMBEAU_CVBS-SWITCH
B08A (1×)	REGIMBEAU_CVBS-SWITCH
B04A (2×)	RESET-AUDIO
B04M (2×)	RESET-AUDIO
B04N (1×)	RESET-BOLT-ON
B07F (1×)	RESET-BOLT-ON
B04A (2×)	RESET-ETHERNET
B07G (2×)	RESET-ETHERNET
B09A (1×)	RESET-ETHERNET
B09A (2×)	RESET-mPCI
B04A (3×)	RESET-NVM
B04A (2×)	RESET-PNX5100
B05F (1×)	RESET-PNX5100
B04A (2×)	RESET-STBY
B02B (1×)	RESET-SYSTEM
B04A (2×)	RESET-SYSTEM
B04B (1×)	RESET-SYSTEM
B04E (1×)	RESET-SYSTEM
B02A (4×)	RF-AGC
B02B (1×)	RF-AGC
B10 (3×)	RIGHT-SPEAKER
B04H (1×)	RREF-PNX85XX
B04P (2×)	RREF-PNX85XX
B04K (1×)	R-VGA
B08B (1×)	R-VGA
B05B (1×)	RX51001A-
B06D (3×)	RX51001A-
B05B (1×)	RX51001A+
B06D (3×)	RX51001A+
B05B (1×)	RX51001B-
B06D (3×)	RX51001B-
B05B (1×)	RX51001B+
B06D (3×)	RX51001B+
B05B (1×)	RX51001C-
B06D (3×)	RX51001C-
B05B (1×)	RX51001C+
B06D (3×)	RX51001C+
B05B (1×)	RX51001CLK-
B06D (3×)	RX51001CLK-
B05B (1×)	RX51001CLK+
B06D (3×)	RX51001CLK+
B05B (1×)	RX51001D-
B06D (3×)	RX51001D-
B05B (1×)	RX51001D+
B06D (3×)	RX51001D+
B05B (1×)	RX51001E-
B06D (3×)	RX51001E-
B05B (1×)	RX51001E+
B06D (3×)	RX51001E+
B05B (1×)	RX51002A-
B06D (3×)	RX51002A-
B05B (1×)	RX51002A+
B06D (3×)	RX51002A+
B05B (1×)	RX51002B-
B06D (3×)	RX51002B-
B05B (1×)	RX51002B+
B06D (3×)	RX51002B+
B05B (1×)	RX51002C-
B06D (3×)	RX51002C-
B05B (1×)	RX51002C+
B06D (3×)	RX51002C+
B05B (1×)	RX51002CLK-
B06D (3×)	RX51002CLK-
B05B (1×)	RX51002CLK+
B06D (3×)	RX51002CLK+
B05B (1×)	RX51002D-
B06D (3×)	RX51002D-
B05B (1×)	RX51002D+
B06D (3×)	RX51002D+
B05B (1×)	RX51002E-
B06D (3×)	RX51002E-
B05B (1×)	RX51002E+
B06D (3×)	RX51002E+
B08D (3×)	RXD
B04E (2×)	RXD-MIPS
B08D (3×)	RXD-MIPS
B04E (2×)	RXD-MIPS2
B06B (1×)	RXD-MIPS2
B04A (2×)	RXD-UP
B08D (4×)	RXD-UP
B04E (2×)	SCL1
B04E (3×)	SCL2
B04E (2×)	SCL3
B05F (1×)	SCL-AMBI-3V3
B06A (1×)	SCL-AMBI-3V3
B06G (1×)	SCL-AMBI-3V3
B04N (1×)	SCL-BOLT-ON
B06A (3×)	SCL-BOLT-ON
B08D (1×)	SCL-BOLT-ON
B05E (2×)	SCL-DISP
B06A (3×)	SCL-DISP
B06D (1×)	SCL-DISP
B01B (1×)	SCL-SET
B04E (2×)	SCL-SET
B06A (5×)	SCL-SET
B06C (2×)	SCL-SET
B06A (2×)	SCL-SET0
B06A (2×)	SCL-SET1
B02B (2×)	SCL-SSB
B04E (2×)	SCL-SSB
B05F (2×)	SCL-SSB
B06A (1×)	SCL-SSB
B06G (1×)	SCL-SSB
B07D (1×)	SCL-SSB
B08D (1×)	SCL-SSB
B04A (3×)	SCL-UP-MIPS
B04E (3×)	SCL-UP-MIPS
B04E (2×)	SDA1
B04E (3×)	SDA2
B04E (2×)	SDA3
B05F (1×)	SDA-AMBI-3V3
B06A (1×)	SDA-AMBI-3V3
B06G (1×)	SDA-AMBI-3V3
B04N (1×)	SDA-BOLT-ON
B06A (3×)	SDA-BOLT-ON
B08D (1×)	SDA-BOLT-ON
B05E (2×)	SDA-DISP
B06A (3×)	SDA-DISP
B06D (1×)	SDA-DISP
B01B (1×)	SDA-SET
B04E (2×)	SDA-SET
B06A (5×)	SDA-SET
B06C (2×)	SDA-SET
B06A (2×)	SDA-SET0
B06A (2×)	SDA-SET1
B02B (2×)	SDA-SSB
B04E (2×)	SDA-SSB
B05F (2×)	SDA-SSB
B06A (1×)	SDA-SSB
B06G (1×)	SDA-SSB
B07D (1×)	SDA-SSB
B08D (1×)	SDA-SSB
B04A (3×)	SDA-UP-MIPS
B04E (3×)	SDA-UP-MIPS
B04A (2×)	SDM
B04B (1×)	SDM
B04P (2×)	SENSE+1V2-PNX85XX
B04L (1×)	SPDIF-IN1
B08D (1×)	SPDIF-IN1
B04L (1×)	SPDIF-OUT
B08B (1×)	SPDIF-OUT
B04A (2×)	SPI-CLK
B04A (2×)	SPI-CSB
B04A (2×)	SPI-PROG
B04B (1×)	SPI-PROG
B04A (3×)	SPI-SDI
B04A (2×)	SPI-SDO
B04A (3×)	SPI-WP
B01B (1×)	STANDBY
B04A (2×)	STANDBY
B08D (1×)	STANDBY
B04A (2×)	SUPPLY-FAULT
B06C (2×)	TACHO1
B06C (2×)	TACHO1-INV
B06C (2×)	TACHO2
B06C (2×)	TACHO2-INV
B06E (1×)	TCK
B06G (1×)	TCK
B06E (1×)	TDI
B06G (1×)	TDI
B06E (1×)	TDO
B06G (1×)	TDO
B06E (1×)	TMS
B06G (1×)	TMS
B04N (2×)	TSINO-DATA0
B07F (1×)	TSINO-DATA0
B04N (2×)	TSINO-DATA1
B07F (1×)	TSINO-DATA1
B04N (2×)	TSINO-DATA2
B07F (1×)	TSINO-DATA2
B04N (2×)	TSINO-DATA3
B07F (1×)	TSINO-DATA3
B04N (2×)	TSINO-DATA4
B07F (1×)	TSINO-DATA4
B04N (2×)	TSINO-DATA5
B07F (1×)	TSINO-DATA5
B04N (2×)	TSINO-DATA6
B07F (1×)	TSINO-DATA6
B04N (2×)	TSINO-DATA7
B07F (1×)	TSINO-DATA7
B04N (2×)	TSO-BIT-CLK
B07F (1×)	TSO-BIT-CLK
B04N (2×)	TSO-BIT-ERR
B04N (2×)	TSO-BIT-VALID
B07F (1×)	TSO-BIT-VALID
B04N (2×)	TSO-SYNC
B07F (1×)	TSO-SYNC
B02A (5×)	TUN-P1
B02A (5×)	TUN-P10
B02A (4×)	TUN-P11
B02A (5×)	TUN-P2
B02A (6×)	TUN-P3
B02A (5×)	TUN-P4
B02A (5×)	TUN-P5
B02A (5×)	TUN-P6
B02A (5×)	TUN-P7
B02A (5×)	TUN-P8
B02A (6×)	TUN-P9
B02A (2×)	TUN-SCL
B02B (2×)	TUN-SCL
B02A (2×)	TUN-SDA
B02B (2×)	TUN-SDA
B05E (3×)	TX1A-
B05E (3×)	TX1A+
B05E (3×)	TX1B-
B05E (3×)	TX1B+
B05E (3×)	TX1C-
B05E (3×)	TX1C+
B05E (3×)	TX1CLK-
B05E (3×)	TX1CLK+
B05E (3×)	TX1D-
B05E (3×)	TX1D+
B05E (3×)	TX1E-
B05E (3×)	TX1E+
B05E (3×)	TX2A-
B05E (3×)	TX2A+
B05E (3×)	TX2B-
B05E (3×)	TX2B+
B05E (3×)	TX2C-
B05E (3×)	TX2C+
B05E (3×)	TX2CLK-
B05E (3×)	TX2CLK+
B05E (3×)	TX2D-
B05E (3×)	TX2D+
B05E (3×)	TX2E-
B05E (3×)	TX2E+
B05E (3×)	TX3A-
B05E (3×)	TX3A+
B05E (3×)	TX3B-
B05E (3×)	TX3B+
B05E (3×)	TX3C-
B05E (3×)	TX3C+
B05E (3×)	TX3CLK-
B05E (3×)	TX3CLK+
B05E (3×)	TX3D-
B05E (3×)	TX3D+
B05E (3×)	TX3E-
B05E (3×)	TX3E+
B05E (3×)	TX4A-
B05E (3×)	TX4A+
B05E (3×)	TX4B-
B05E (3×)	TX4B+
B05E (3×)	TX4C-
B05E (3×)	TX4C+
B05E (3×)	TX4CLK-
B05E (3×)	TX4CLK+
B05E (3×)	TX4D-
B05E (3×)	TX4D+
B05E (3×)	TX4E-
B05E (3×)	TX4E+
B04O (1×)	TX851A-
B06D (1×)	TX851A-
B06G (1×)	TX851A-
B04O (1×)	TX851A+
B06D (1×)	TX851A+
B06G (1×)	TX851A+
B04O (1×)	TX851B-
B06D (1×)	TX851B-
B06G (1×)	TX851B-
B04O (1×)	TX851B+
B06D (1×)	TX851B+
B06G (2×)	TX851B+
B04O (1×)	TX851C-
B06D (1×)	TX851C-
B06G (1×)	TX851C-
B04O (1×)	TX851C+
B06D (1×)	TX851C+
B06G (1×)	TX851C+
B04O (1×)	TX851CLK-
B06D (1×)	TX851CLK-
B06G (1×)	TX851CLK-
B04O (1×)	TX851CLK+
B06D (1×)	TX851CLK+
B06G (1×)	TX851CLK+
B04O (1×)	TX851D-
B06D (1×)	TX851D-
B06G (1×)	TX851D-
B04O (1×)	TX851D+
B06D (1×)	TX851D+
B06G (1×)	TX851D+
B04O (1×)	TX851E-
B06D (1×)	TX851E-
B06G (1×)	TX851E-
B04O (1×)	TX851E+
B06D (1×)	TX851E+
B06G (1×)	TX851E+
B04O (1×)	TX852A-
B06D (1×)	TX852A-
B06G (1×)	TX852A-
B04O (1×)	TX852A+
B06D (1×)	TX852A+
B06G (1×)	TX852A+
B04O (1×)	TX852B-
B06D (1×)	TX852B-
B06G (1×)	TX852B-
B04O (1×)	TX852B+
B06D (1×)	TX852B+
B06G (1×)	TX852B+
B04O (1×)	TX852C-
B06D (1×)	TX852C-
B06G (1×)	TX852C-
B04O (1×)	TX852C+
B06D (1×)	TX852C+
B06G (1×)	TX852C+
B04O (1×)	TX852CLK-
B06D (1×)	TX852CLK-
B06G (1×)	TX852CLK-
B04O (1×)	TX852CLK+
B06D (1×)	TX852CLK+
B06G (1×)	TX852CLK+
B04O (1×)	TX852D-
B06D (1×)	TX852D-
B06G (1×)	TX852D-
B04O (1×)	TX852D+
B06D (1×)	TX852D+
B06G (1×)	TX852D+
B04O (1×)	TX852E-
B06D (1×)	TX852E-
B06G (1×)	TX852E-
B04O (1×)	TX852E+
B06D (1×)	TX852E+
B06G (1×)	TX852E+
B05E (1×)	TXCLK-
B06A (1×)	TXCLK-
B05E (1×)	TXCLK+
B06A (1×)	TXCLK+
B08D (3×)	TXD
B05E (1×)	TXDAT-
B06A (1×)	TXDAT-
B05E (1×)	TXDAT+
B06A (1×)	TXDAT+
B04E (2×)	TXD-MIPS
B08D (3×)	TXD-MIPS
B04E (2×)	TXD-MIPS2
B06B (1×)	TXD-MIPS2
B04A (2×)	TXD-UP
B08D (4×)	TXD-UP
B06D (1×)	TXF1A-
B06G (1×)	TXF1A-
B06D (1×)	TXF1A+
B06G (1×)	TXF1A+
B06D (1×)	TXF1B-
B06G (1×)	TXF1B-
B06D (1×)	TXF1B+
B06G (1×)	TXF1B+
B06D (1×)	TXF1C-
B06G (1×)	TXF1C-
B06D (1×)	TXF1C+
B06G (1×)	TXF1C+
B06D (1×)	TXF1CLK-
B06G (1×)	TXF1CLK-
B06D (1×)	TXF1CLK+
B06G (1×)	TXF1CLK+
B06D (1×)	TXF1D-
B06G (1×)	TXF1D-
B06D (1×)	TXF1D+
B06G (1×)	TXF1D+
B06D (1×)	TXF1E-
B06G (1×)	TXF1E-
B06D (1×)	TXF1E+
B06G (1×)	TXF1E+
B06D (1×)	TXF2A-
B06G (1×)	TXF2A-
B06D (1×)	TXF2A+
B06G (1×)	TXF2A+
B06D (1×)	TXF2B-
B06G (1×)	TXF2B-
B06D (1×)	TXF2B+
B06G (1×)	TXF2B+
B06D (1×)	TXF2C-
B06G (1×)	TXF2C-
B06D (1×)	TXF2C+
B06G (1×)	TXF2C+
B06D (1×)	TXF2CLK-
B06G (1×)	TXF2CLK-
B06D (1×)	TXF2CLK+
B06G (1×)	TXF2CLK+
B06D (1×)	TXF2D-
B06G (1×)	TXF2D-
B06D (1×)	TXF2D+
B06G (1×)	TXF2D+
B06D (1×)	TXF2E-
B06G (1×)	TXF2E-
B06D (1×)	TXF2E+
B06G (1×)	TXF2E+
B04A (2×)	UART-SWITCH
B08D (2×)	UART-SWITCH
B08D (2×)	UART-SWITCHn
B04E (2×)	USB20-DM
B07C (1×)	USB20-DM
B04E (2×)	USB20-DP
B07C (1×)	USB20-DP
B04E (1×)	USB-OC
B07C (1×)	USB-OC
B04P (2×)	VDDA-ADC
B04L (4×)	VDDA-AUDIO
B04P (2×)	VDDA-AUDIO
B04L (1×)	VDDA-DAC
B04P (2×)	VDDA-DAC
B04O (1×)	VDDA-LVDS
B04P (1×)	VDDA-LVDS
B06F (2×)	VREF-DDR1
B06F (1×)	VREF-FPGA1
B06G (16×)	VREF-FPGA1
B01A (1×)	VSW
B01B (1×)	VSW
B04K (1×)	V-SYNC-VGA
B08B (1×)	V-SYNC-VGA
B04E (1×)	WC-EEPROM-PNX5100
B05F (2×)	WC-EEPROM-PNX5100
B07D (1×)	WC-EEPROM-PNX5100
B04A (2×)	WP-NANDFLASH
B07F (2×)	WP-NANDFLASH
B07D (1×)	WRITE-PROT
B07E (1×)	WRITE-PROT
B08B (1×)	WRITE-PROT
B04F (1×)	XIO-ACK
B07F (2×)	XIO-ACK
B04F (1×)	XIO-SEL-NAND
B07F (2×)	XIO-SEL-NAND
B04K (1×)	Y_CVBS-MON-OUT
B08B (1×)	Y_CVBS-MON-OUT
B08A (1×)	Y_CVBS-MON-OUT-SC
B08B (1×)	Y_CVBS-MON-OUT-SC

3104 313 6343.2

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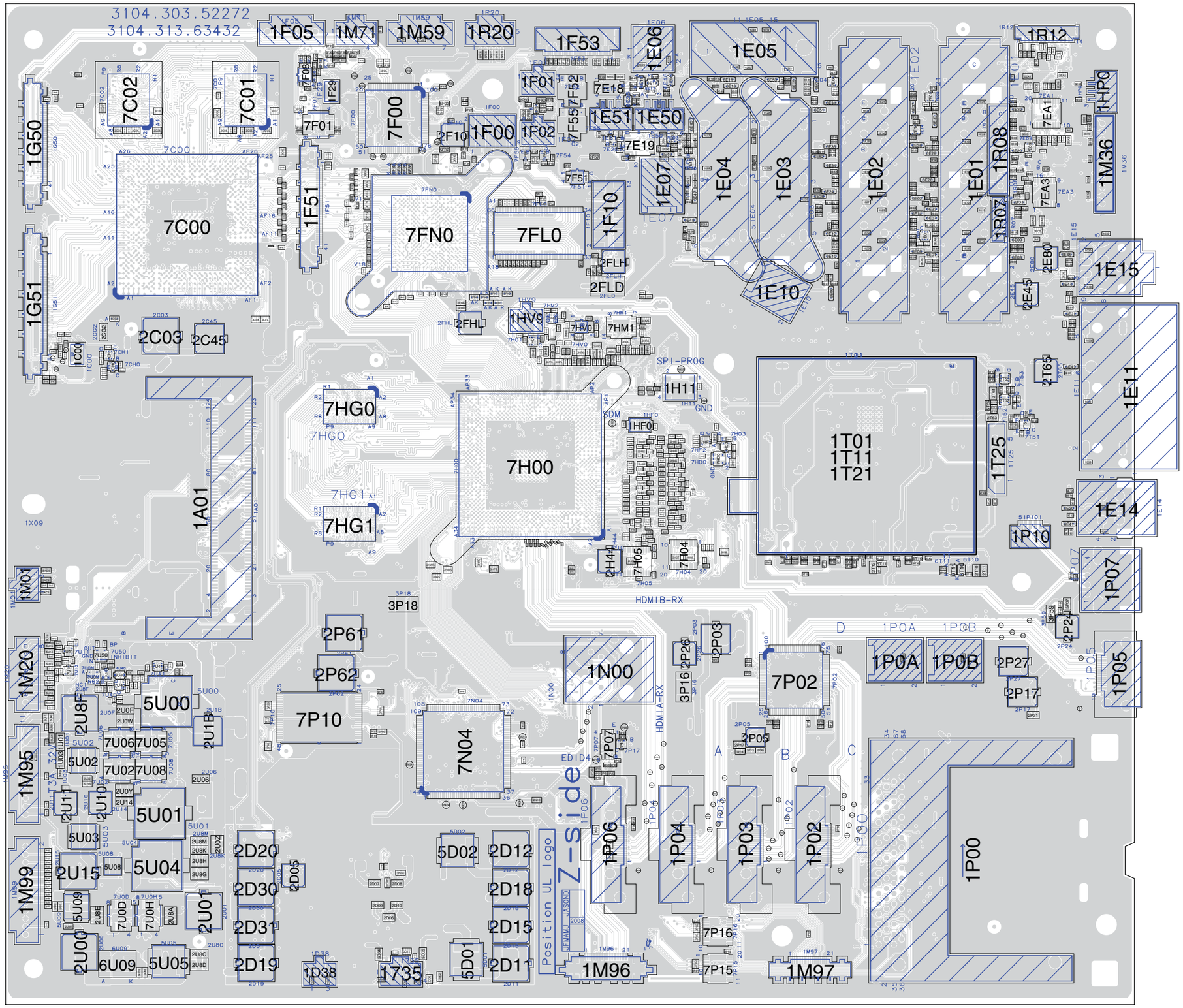
090309

Layout Small Signal Board (Top Side)



3104 313 6343.2

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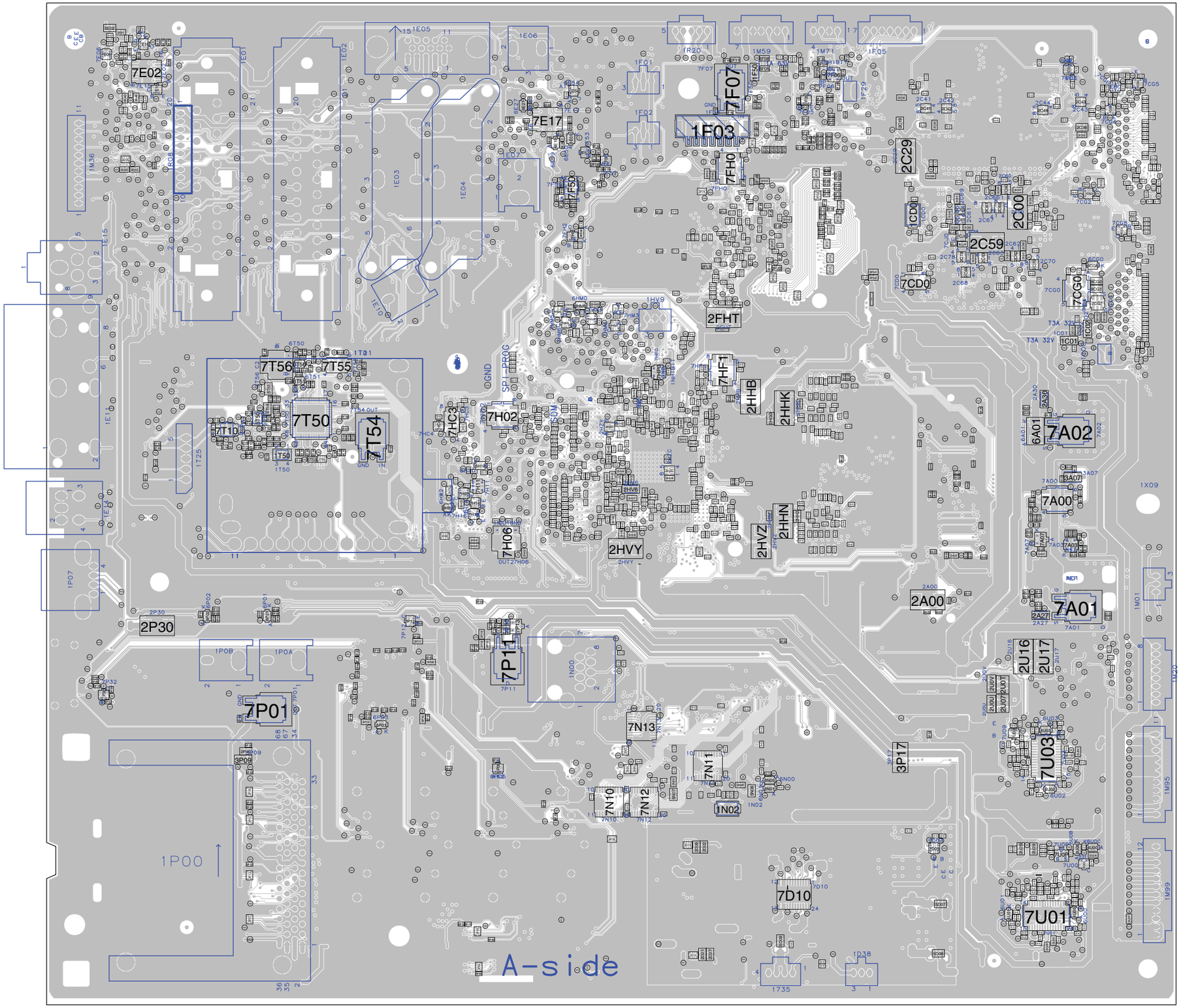
Layout Small Signal Board (Bottom Side)



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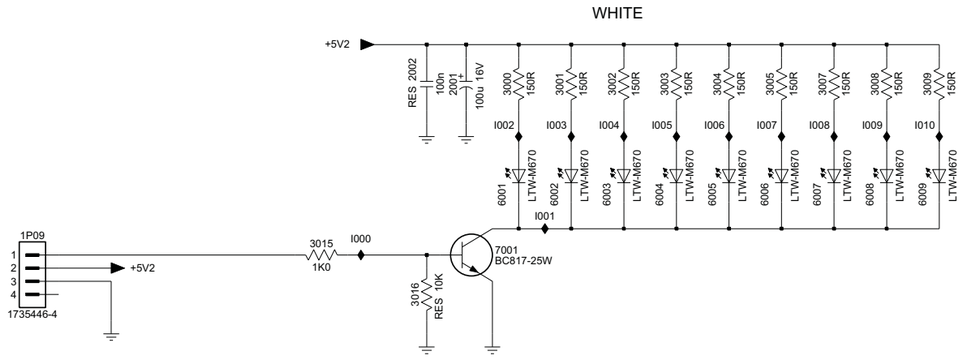
Light guide

LIGHT GUIDE



1P09 C1
2001 B4
2002 B3
3000 B4
3001 B4
3002 B4
3003 B5
3004 B5
3005 B5
3007 B6
3008 B6
3009 B6
3015 C3
3016 C3
6001 B4
6002 B4
6003 B4
6004 B5
6005 B5
6006 B5
6007 B6
6008 B6
6009 B6
7001 C4
I000 C3
I001 C4
I002 B4
I003 B4
I004 B4
I005 B5
I006 B5
I007 B5
I008 B6
I009 B6
I010 B6

CHN	SETNAME 2K9		
CLASS_NO	LIGHT STRIP PANEL 9 LEDS 2K9	3104 313 6344	1 2008-10-16
2008-10-17 3			
NAME Luc Buffel	SUPERS. 1	130 – 1	A3
CHECK	DATE		

18310_560_090508.eps
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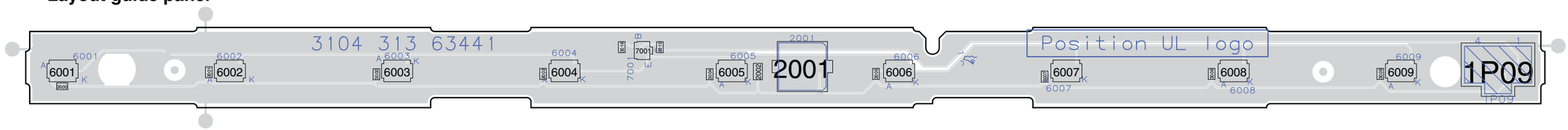
Layout guide panel



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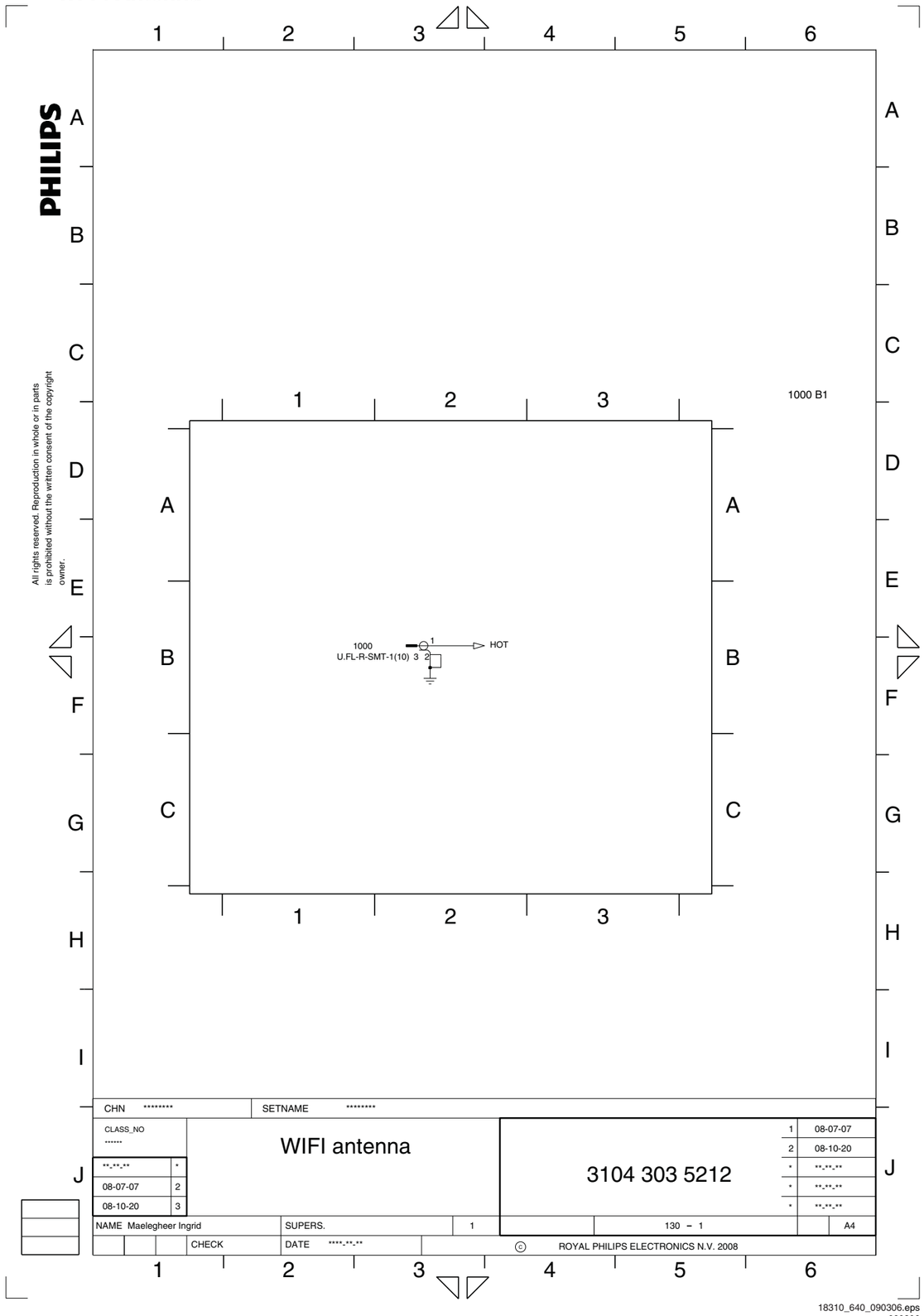
Wi-Fi Antenna



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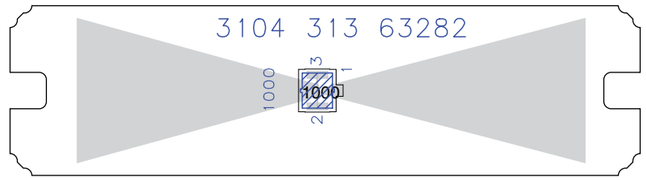
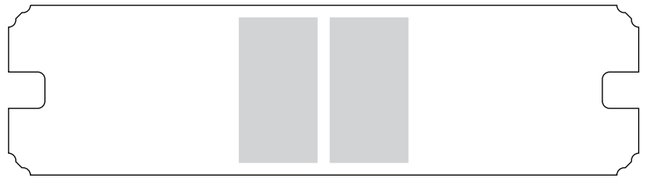
Layout Wi-Fi Antenna





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